HC32F460 series

32-bit ARM ® Cortex ® -M4 Microcontroller

HC32F460PETB-LQFP100 / HC32F460PEHB-VFBGA100

HC32F460KETA-LQFP64 / HC32F460KEUA-QFN60TR

HC32F460JETA-LQFP48 / HC32F460JEUA-QFN48TR

HC32F460PCTB-LQFP100 / HC32F460KCTA-LQFP64

HC32F460JCTA-LQFP48

Datasheet

Features

ARM Cortex-M4 32bit MCU+FPU, 250DMIPS, up to 512KB Flash, 192KB SRAM, USB FS (Device/Host), 14 Timers, 2 ADCs, 1 PGA, 3 CMPs, 20 communication interfaces

- ARMv7-M architecture 32bit Cortex-M4 CPU, integrated FPU, MPU, DSP supporting SIMD instructions, and CoreSight standard debugging unit. The highest working frequency is 200MHz, and the Flash acceleration unit realizes 0-wait program execution, reaching the computing performance of 250DMIPS or 680Coremarks
- Built-in memory
  - Flash memory up to 512KByte, supports security protection and data encryption [*1]
  - Maximum 192KByte SRAM, including 32KByte 200MHz single-cycle access high-speed RAM, 4KByte Retention RAM
- Power, Clock, Reset Management
  - System power supply (Vcc): 1.8-3.6V
  - 6 independent clock sources: External main clock crystal (4-25MHz), external secondary crystal (32.768kHz), internal high-speed RC (16/20MHz), internal medium-speed RC (8MHz), internal low-speed RC (32kHz), internal WDT dedicated RC (10kHz)
  - 14 kinds of reset sources including power-on reset (POR), low voltage detection reset (LVDR), port reset (PDR), each reset source has an independent flag bit
- Low power operation
  - Peripherals can be turned off or on independently
  - Three low power consumption modes: Sleep, Stop, Power down mode
  - Supports switching between ultra-high-speed mode, high-speed mode, and ultra-low-speed mode in Run mode and Sleep mode
  - Standby power consumption: Stop mode typ.90uA@25°C, Power down mode is as low as 1.8uA@25°C
  - In Power down mode, support 16 ports to wake up, support ultra-low power RTC work, 4KByte SRAM to hold data
  - Standby wakes up quickly, Stop mode wakes up as fast as 2us, Power down mode wakes up as fast as 20us
- Peripheral operation support system significantly reduces CPU processing load
  - 8-channel dual-host DMAC
  - USBFS dedicated DMAC
  - Data Calculation Unit (DCU)
  - Supports mutual triggering of peripheral events (AOS)
- High-performance simulation
  - 2 independent 12bit 2MSPS ADC
  - 1 programmable gain amplifier (PGA)
  - 3 independent voltage comparators (CMP), supporting 2 internal reference voltages
  - 1 on-chip temperature sensor (OTS)
- Timer
  - 3 multi-function 16bit PWM Timer (Timer6)
  - 3 16-bit motor PWM Timers (Timer4)
  - 6 16bit universal Timer (TimerA)
  - 2 16bit basic Timer (Timer0)
- Maximum 83 GPIO
  - CPU single cycle access, maximum 100MHz output
  - Maximum 81 5V-tolerant IO
- Maximum 20 communication interfaces
  - 3 I2C, support SMBus protocol
  - 4 USART, support ISO7816-3 protocol
  - 4 SPI
  - 4 I2S, built-in audio PLL to support audio-level sampling accuracy
  - 2 SDIO, support SD/MMC/eMMC format
  - 1 QSPI, support 200Mbps high-speed access (XIP)
  - 1 CAN, supporting ISO11898-1 standard

protocol

– 1 USB 2.0 FS, built-in PHY, support Device/Host

- Data encryption function
  – AES/HASH/TRNG
- Encapsulation form:
  LQFP100 (14×14mm) VFBGA100 (7×7mm)
  LQFP64 (10×10mm) QFN60 (7×7mm)
  QFN48 (5×5mm) LQFP48 (7×7mm)

**1: For the specific specifications of Flash security protection and data encryption, please consult the sales window.*

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Table of Contents

List of Tables

List of Figures

1 Overview

The HC32F460 series is a high-performance MCU based on ARM® Cortex®-M4 32-bit RISC CPU with a maximum operating frequency of 200MHz. The Cortex-M4 core integrates a floating-point arithmetic unit (FPU) and a DSP to implement single-precision floating-point arithmetic operations, supports all ARM single-precision data processing instructions and data types, and supports the complete DSP instruction set. The kernel integrates the MPU unit and superimposes the DMAC dedicated MPU unit at the same time to ensure the safety of system operation.

The HC32F460 series integrates high-speed on-chip memory, including Flash up to 512KB and SRAM up to 192KB. Integrated Flash access acceleration unit to achieve single cycle program execution of the CPU on Flash. The polled bus matrix supports multiple bus hosts to access memory and peripherals simultaneously, improving performance. The bus host includes CPU, DMA, USB dedicated DMA, etc. In addition to the bus matrix, it supports data transfer between peripherals, and basic arithmetic operations and events trigger each other, which can significantly reduce the transaction processing load of the CPU.

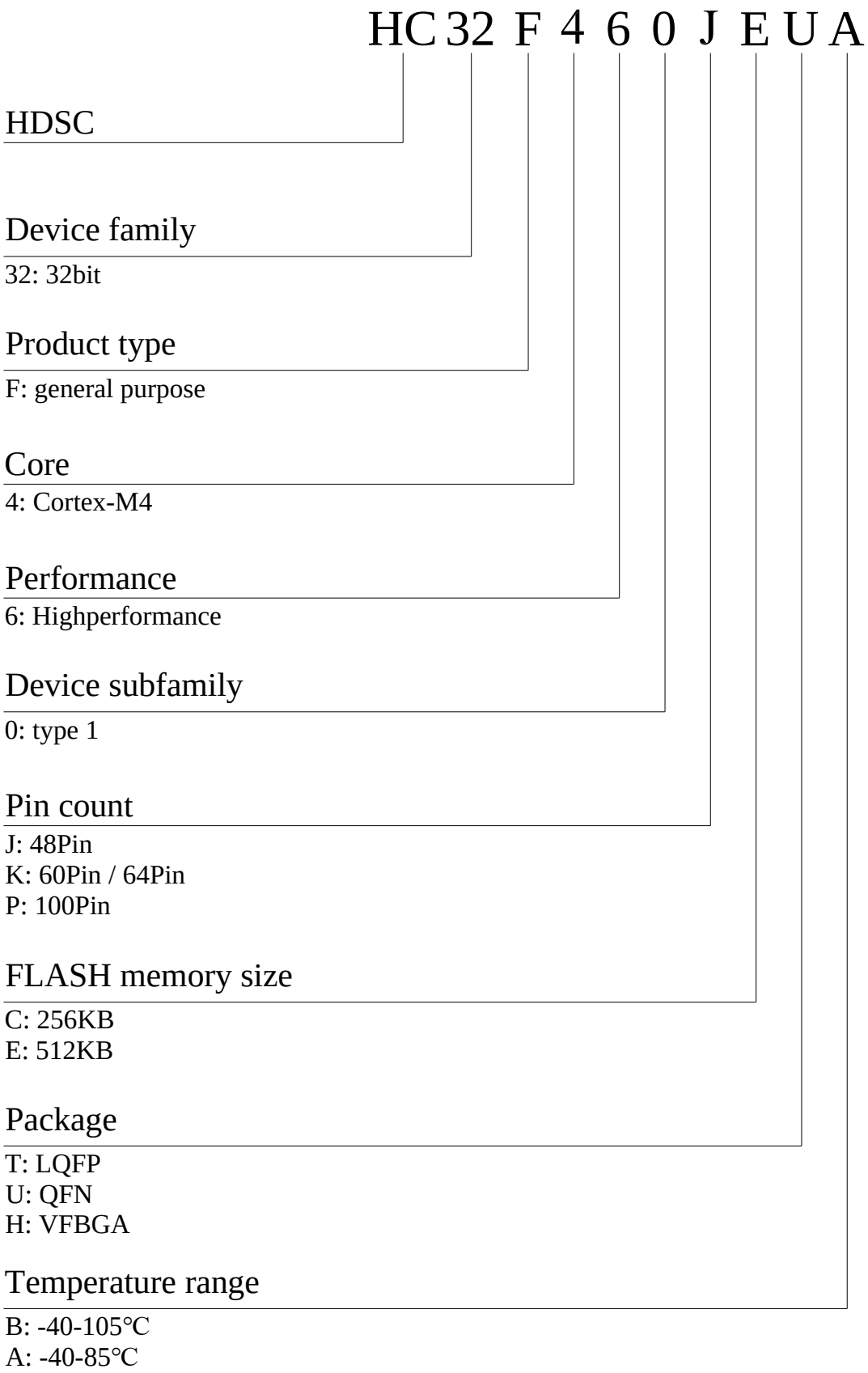
The HC32F460 series integrates a wealth of peripheral functions. Including 2 independent 12bit 2MSPS ADCs, 1 gain adjustable PGA, 3 voltage comparators (CMP), 3 multifunctional 16bit PWM Timers (Timer6) support 6 complementary PWM outputs, 3 motor PWM Timers (Timer4) Support 18 complementary PWM outputs, 6 16bit general-purpose Timers (TimerA), 3 3-phase quadrature encoding inputs and 48 Duty independent programmable PWM outputs, 11 serial communication interfaces (I2C/UART/SPI), 1 QSPI interface, 1 CAN, 4 I2S support audio PLL, 2 SDIO, 1 USB FS Controller with on-chip FS PHY to support Device/Host.

The HC32F460 series supports a wide voltage range (1.8-3.6V), a wide temperature range (-40-105°C) and various low power consumption modes. Super-high-speed mode (≤200MHz), high-speed mode (≤168MHz) and ultra-low-speed mode (≤8MHz) can be switched in Run mode and Sleep mode. Supports fast wake-up in low-power mode, STOP mode wake-up as fast as 2us, Power Down mode wake-up as fast as 20us.

Typical application

HC32F460 series provide 48pin, 64pin, 100pin LQFP package, 48pin, 60pin QFN package, 100pin of VFBGA Package, It is suitable for high-performance motor frequency conversion control, intelligent hardware, IoT connection modules and other fields.

1.1 Part naming rules



1.2 Part function comparison table

Function		Product								
		HC32F460PEHB	HC32F460PETB	HC32F460PCTB	HC32F460KETA	HC32F460KCTA	HC32F460JETA	HC32F460JCTA	HC32F460JEUA	HC32F460KEUA
Flash Memory (KB)		512	512	256	512	256	512	256	512	512
Pin number		100	100	100	64	64	48	48	48	60
Number of GPIOs		83	83	83	52	52	38	38	38	50
5V Tolerant GPIO number		81	81	81	50	50	36	36	36	48
Pin Pitch		VFBGA	LQFP						QFN	
Temperature range		-40-105℃			-40-85℃					
Supply voltage range		1.8 ~ 3.6 V								
OTP (Byte)		960								
SRAM (KB)		192								
DMA		2unit * 4ch								
External port interrupt		EIRQ * 16vec + NMI * 1ch								
Communcation Interfaces (In the parentheses is the minimum number of IOs required for each ch)	UART	4ch (2)								
	SPI	4ch (3)								
	I2C	3ch (2)								
	I2S	4ch (3)								
	CAN	1ch (2)								
	QSPI	1ch (6)								
	SDIO	2ch (3)								
	USB-FS	1ch (2)								
Timers	Timer0	2unit								
	TimerA	6unit								
	Timer4	3unit								
	Timer6	3unit								
	WDT	1ch								
	SWDT	1ch								
	RTC	1ch								
Analog	12bit ADC	2unit, 16ch					2unit, 10ch			2unit, 15ch
	PGA	1ch								
	CMP	3ch								
	OTS	√								

AES128	√
HASH (SHA256)	√
TRNG	√
Frequency Monitoring Module	√
Programmable voltage	√
Debug interface	SWD
	JTAG

Table 1 - 1 Model function comparison table

1.3 Functional block diagram

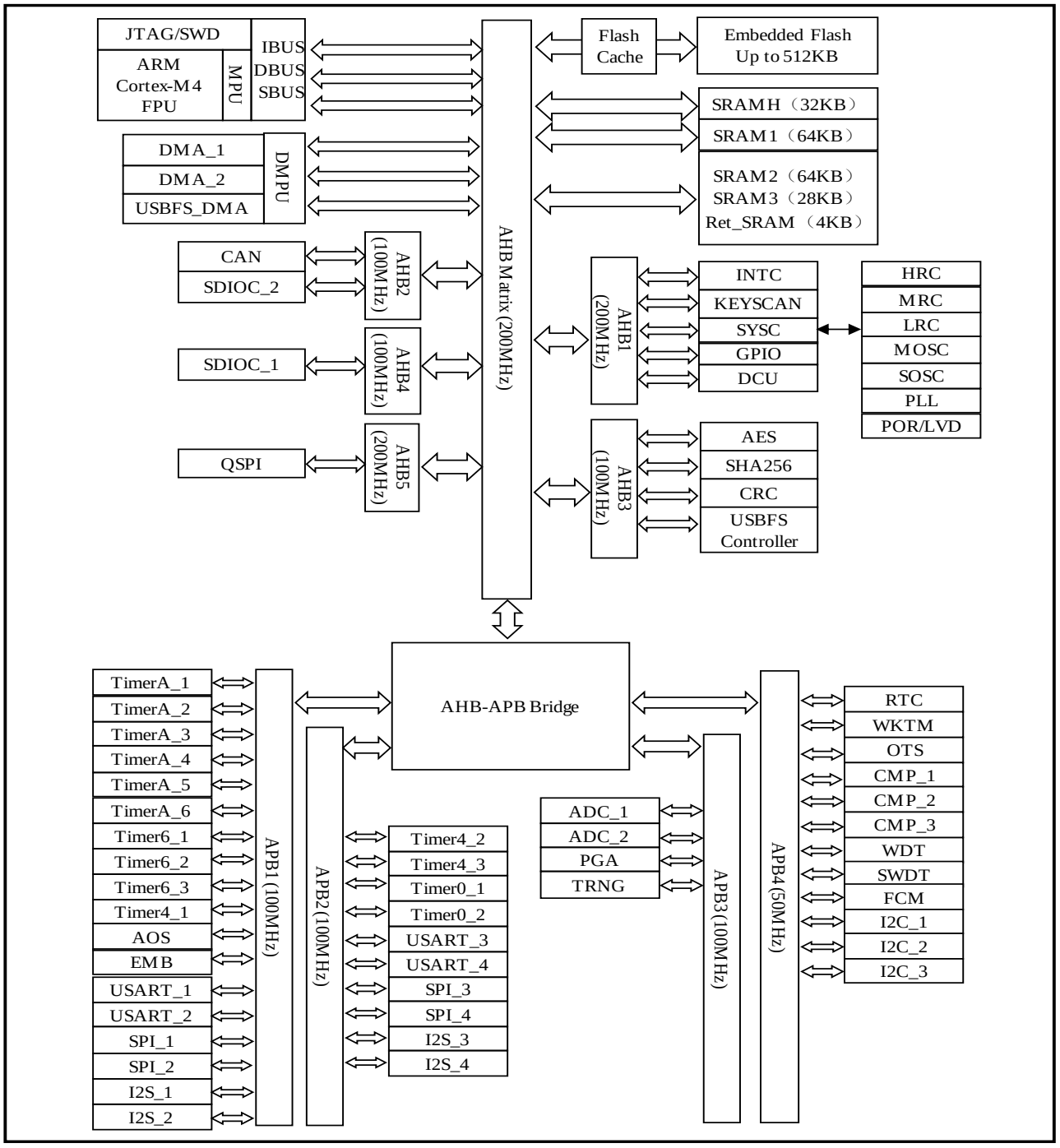


Figure 1 -1 Functional block diagram

1.4 Feature Brief

1.4.1 CPU

The HC32F460 series integrates the latest generation of embedded ARM® Cortex®-M4 with FPU 32bit streamlined instruction CPU, achieving low pins and low power consumption, while providing excellent computing performance and rapid interrupt response capabilities. The on-chip integrated storage capacity can give full play to the excellent instruction efficiency of ARM® Cortex®-M4 with FPU. The CPU supports DSP instructions, which can realize efficient signal processing operations and complex algorithms. Single-point precision FPU (Floating Point Unit) unit can avoid instruction saturation and speed up software development.

1.4.2 Bus Architecture (BUS)

The main system is composed of a 32-bit multi-layer AHB bus matrix, which can realize the interconnection of the following host bus and slave bus.

Host bus

- Cortex-M4F core CPU-I bus, CPU-D bus, CPU-S bus
- System DMA_1 bus, system DMA_2 bus
- USBFS_DMA bus

Slave bus

- Flash ICODE bus
- Flash DCODE bus
- Flash MCODE bus (the bus used by hosts other than the CPU to access Flash)
- SRAMH bus (SRAMH 32kB)
- SRAMA bus (SRAM1 64KB)
- SRAMB bus (SRAM2 64KB, SRAM3 28KB, Ret_SRAM 4KB)
- APB1 peripheral bus (AOS/EMB/Timers/SPI/USART/I2S)
- APB2 peripheral bus (Timers/SPI/USART/I2S)
- APB3 peripheral bus (ADC/PGA/TRNG)
- APB4 peripheral bus (FCM/WDT/CMP/OTS/RTC/WKTM/I2C)

- AHB1 peripheral bus (KEYSCAN/INTC/DCU/GPIO/SYSC)
- AHB2 Peripheral Bus (CAN/SDIOC)
- AHB3 peripheral bus (AES/HASH/CRC/USB FS)
- AHB4 Peripheral Bus (SDIOC)
- AHB5 Peripheral Bus (QSPI)

With the help of the bus matrix, high-efficiency concurrent access from the host bus to the slave bus can be realized.

1.4.3 Reset control (RMU)

The chip is configured with 14 reset modes.

- Power-on Reset (POR)
- NRST pin reset (NRST)
- Brown-out reset (BOR)
- Programmable voltage detection 1 reset (PVD1R)
- Programmable voltage detection 2 reset (PVD2R)
- Watchdog reset (WDTR)
- Special watchdog reset (SWDTR)
- Power-down wake-up reset (PDRST)
- Software Reset (SRST)
- MPU error reset (MPUR)
- RAM parity reset (RAMPR)
- RAMECC reset (RAMECCR)
- Clock abnormal reset (CKFER)
- External High Speed Oscillator Abnormal Shock Reset (XTALER)

1.4.4 Clock control (CMU)

The clock control unit provides a series of frequency clock functions, including: One external high-speed oscillator, one external low-speed oscillator, two PLL clocks, one internal high-speed oscillator, one internal medium-speed oscillator, one internal low-speed oscillator, one

SWDT dedicated internal low-speed oscillator, clock prescaler, Clock multiplexing and clock gating circuit.

The clock control unit also provides a clock frequency measurement function. The clock frequency measurement circuit (FCM) uses the measurement reference clock to monitor and measure the measurement target clock. An interrupt or reset occurs when the setting range is exceeded.

The AHB, APB and Cortex-M4 clocks are all derived from the system clock, and the source of the system clock can be selected from 6 clock sources:

1) External high-speed oscillator (XTAL)
2) External low-speed oscillator (XTAL32)
3) MPLL clock (MPLL)
4) Internal high-speed oscillator (HRC)
5) Internal Medium Speed Oscillator (MRC)
6) Internal low-speed oscillator (LRC)

The maximum operating clock frequency of the system clock can reach 200MHz. SWDT has an independent clock source: SWDT dedicated internal low-speed oscillator (SWDTLRC). The real-time clock (RTC) uses an external low-speed oscillator or an internal low-speed oscillator as the clock source. The 48MHz clock and I2S communication clock of USB-FS can choose the system clock, MPLL, UPLL as the clock source.

For each clock source, it can be turned on and off individually. It is recommended to turn off unused clock sources to reduce power consumption.

1.4.5 Power control (PWC)

Power controller is used to control the supply, switching and detection of multiple power domains in multiple operation modes and low power modes. The power controller is composed of power consumption control logic (PWCL) and power supply voltage detection unit (PVD). The operating voltage (VCC) of the chip is 1.8V to 3.6V. The voltage regulator (LDO) supplies power to the VDD domain and the VDDR domain, and the VDDR voltage regulator (RLDO) supplies power to the VDDR domain in power-down mode. The chip provides three operating

modes of ultra-high-speed, high-speed, and ultra-low-speed through the power control logic (PWCL), and three low-power modes such as sleep, stop and power-down.

The power supply voltage detection unit (PVD) provides functions such as power-on reset (POR), power-down reset (PDR), brown-out reset (BOR), programmable voltage detection 1 (PVD1), programmable voltage detection 2 (PVD2), etc. Among them, POR, PDR, and BOR control the chip reset action by detecting the VCC voltage. PVD1 can reset or interrupt the chip according to the register setting by detecting the VCC voltage. PVD2 detects the voltage by detecting the VCC voltage or external input, and generates a reset or interrupt according to the register selection.

The VDDR area can maintain power through RLDO after the chip enters the power-down mode to ensure that the real-time clock module (RTC) and wake-up timer (WKTM) can continue to operate, and maintain 4KB of low-power SRAM (Ret-SRAM) data. The analog module is equipped with a dedicated power supply pin, which improves the analog performance.

1.4.6 Initialization Configuration (ICG)

After the chip reset is released, the hardware circuit will read the FLASH address 0x0000_0400~0x0000_041F (where 0x0000_0408~0x0000_041F is the reserved function address, this 24byte address needs to be set by the user to ensure the normal operation of the card) and load the data into the initialization configuration register. The user needs to program or erase FLASH sector 0 to modify the initial configuration register.

1.4.7 Embedded FLASH Interface (EFM)

The FLASH interface accesses FLASH through the ICODE, DCODE and MCODE buses. This interface can perform programming, sector erase and full erase operations on FLASH; speed up code execution through instruction prefetch and cache mechanisms.

Main features:

- Maximum 512KByte FLASH space
- I-CODE bus 16Byte prefetched value
- Shared 64 buffers (1Kbyte) on I-CODE and D-CODE buses

- Provide 960Bbyte one-time programming area (OTP)
- Support low-power read operation
- Support boot exchange function
- Support security protection and data encryption *1

*1: For the specific specifications of Flash security protection and data encryption, please consult the sales window

1.4.8 Built-in SRAM (SRAM)

This product has 4KB power-down mode retention SRAM (Ret_SRAM) and 188KB system SRAM (SRAMH/SRAM1/SRAM2/SRAM3).

SRAM can be accessed by byte, half word (16 bits) or full word (32 bits). Read and write operations are executed at CPU speed, and wait cycles can be inserted.

Ret_SRAM can provide 4KB of data retention space in Power down mode.

SRAM3 has ECC check (Error Checking and Correcting), ECC check is correct one check two code, that can correct one error and check two errors; SRAMH/SRAM1/SRAM2/Ret_SRAM has parity check (Even- parity check), each byte of data has a parity bit.

1.4.9 General IO (GPIO)

Main features of GPIO:

- Each port group has 16 I/O Pins, which may be less than 16 depending on actual configuration
- Support pull-up
- Support push-pull, open-drain output mode
- Support high, medium and low drive modes
- Support for external interrupt input
- Support I/O pin peripheral function multiplexing, each I/O pin up to 16 optional multiplexing functions, some I/O up to 64 functions are optional
- Individual I/O pins can be programmed independently
- Each I/O pin can select 2 functions to be effective at the same time (does not support 2

output functions to be effective at the same time)

1.4.10 Interrupt control (INTC)

The function of the interrupt controller (INTC) is to select an interrupt event request as an interrupt input to the NVIC to wake up WFI; as an event input to wake up WFE. Select interrupt event request as the wake-up condition of low power consumption mode (sleep mode and stop mode); interrupt control function of external pin NMI and EIRQ; interrupt/event selection function of software interrupt.

Main specifications:

1) NVIC interrupt vector: Please refer to the user manual for the actual number of interrupt vectors used (not including the 16 interrupt lines of Cortex™-M4F). Each interrupt vector can select the corresponding peripheral interrupt event request according to the interrupt selection register. For more instructions on exceptions and NVIC programming, please refer to Chapter 5 in the "ARM Cortex™-M4F Technical Reference Manual": Exception and Chapter 8: Nested vectored interrupt controller.
2) Programmable priority: 16 programmable priority levels (4 bit interrupt priority levels are used).
3) Non-maskable interrupt: In addition to the NMI pin as a non-maskable interrupt source, a variety of system interrupt event requests can be independently selected as non-maskable interrupts, and each interrupt event request is equipped with independent enable selection, suspend, and clear suspend registers.
4) Equipped with 16 external pin interrupts.
5) Configure a variety of peripheral interrupt event requests, please refer to the interrupt event request sequence number list for details.
6) Equipped with 32 software interrupt event requests.
7) Interrupt wakes up system sleep mode and stop mode.

1.4.11 Automatic Operation System (AOS)

Automatic Operation System (Automatic Operation System) is used to realize the linkage

between peripheral hardware circuits without the help of CPU. Use the events generated by the peripheral circuit as the AOS source, such as the comparison match of the timer, the timing overflow, the periodic signal of the RTC, the various states of the data transmission and reception of the communication module (idle, receiving data full, sending data end, Send data empty), ADC conversion ends, etc., to trigger the actions of other peripheral circuits. The triggered peripheral circuit action is called AOS Target (AOS Target).

1.4.12 Keyboard scan (KEYSCAN)

This product is equipped with 1 unit of keyboard control module (KEYSCAN). KEYSCAN module supports keyboard array (row and column) scanning, the column is driven by independent scanning output KEYOUTm (m=0~7), and the row KEYINn (n=0~15) is used as EIRQn (n=0~15) input Was detected. This module realizes the key recognition function through the line scan query method.

1.4.13 Storage protection unit (MPU)

The MPU can provide protection for the memory, and by preventing unauthorized access, the security of the system can be improved.

This product has built-in four MPU units for the host and one MPU unit for IP.

Among them, ARM MPU provides CPU access control to the entire 4G address space.

DMA MPU (DMPU) provides DMA_1/DMA_2/USB FS DMA read and write access control for all 4G address spaces. When access to the prohibited space occurs, the MPU action can be set to ignore/bus error/non-maskable interrupt/reset.

IP MPU provides access control to system IP and security-related IP in non-privileged mode.

1.4.14 DMA controller （DMA）

DMA is used to transfer data between memory and peripheral functional modules. It can exchange data between memory, between memory and peripheral functional modules and between peripheral functional modules without CPU involvement.

- DMA bus is independent of CPU bus and transmitted according to AMBA AHB-Lite bus

protocol.

- Has 8 independent channels (DMA_1 and DMA_2 each with 4 channels), which can independently operate different DMA transfer functions
- For each channel, the source of the boot request is configured via a separate trigger source
- One block per request
- The data block is a minimum of one data and can be up to 1024 data
- Each data can be configured to 8 bits, 16 bits or 32 bits
- Up to 65535 transmissions can be configured
- The source address and destination address can be independently configured as fixed, auto-increment, auto-decrement, loop or jump with specified offset
- Three types of interrupts can be generated, block transport complete interrupt, transport complete interrupt, and transport error interrupt. Each interrupt can be configured with a mask or not. Where block transport is complete, transport complete can be used as event output, as trigger source input for other peripheral modules with hardware trigger function
- Support for linked transmission to enable multiple blocks of data to be transmitted at a time
- Support external event trigger channel reset
- You can set the module stop state to reduce power consumption when not in use

1.4.15 Voltage comparator (CMP)

CMP is a peripheral module that compares two analog voltages INP and INM and outputs the comparison result. CMP has 3 independent comparison channels in total, and the analog voltage INP and INM of each comparison channel has 4 input sources. When using, you can select one INP and one INM for single comparison, or you can scan and compare multiple INPs with the same INM. The comparison result can be read through the register, can also be output to an external pin, and can also generate interrupts and events.

1.4.16 Analog-to-digital converter (ADC)

12-bit ADC is an analog-to-digital converter with successive approximation. It has a

maximum of 16 analog input channels, which can convert external ports and internal analog signals. These channels can be arbitrarily combined into a sequence for successive scan conversion, and the sequence can be converted into a single or continuous scan. Support multiple consecutive conversions on any specified channel and average the conversion results. The ADC module also carries the analog watchdog function, monitors the conversion result of any specified channel, and detects whether it exceeds the threshold set by the user.

ADC main characteristics

- High performance
  - Configurable 12-bit, 10-bit and 8-bit resolution
  - The frequency ratio of the peripheral clock PCLK4 and the A/D conversion clock ADCLK can be selected:
    - PCLK4: ADCLK=1:1, 2:1, 4:1, 8:1, 1:2, 1:4
    - ADCLK can choose a PLL asynchronous with the system clock HCLK. At this time, the clock sources of PCLK4 and ADCLK are fixed as PLL at the same time, and the frequency ratio is 1:1, and the original frequency division setting is invalid
  - 2MSPS (PCLK4=ADCLK=60MHz, 12 bits, sampling 17 cycles)
  - Independent programming of the sampling time of each channel
  - Channel-independent data register
  - Data register configurable data alignment
  - Continuous multiple conversion averaging function
  - Simulation watchdog, monitoring conversion results
  - The ADC module can be set to stop when not in use
- Analog input channel
  - Maximum 16 external analog input channels
  - 1 internal reference voltage
- Conversion start condition
  - Software Setup Conversion Started
  - Start of Peripheral Device Synchronization Trigger Conversion

  - External Pin Triggering Start
- Conversion mode
  - 2 scan sequences A and B, optionally specifying a single or multiple channels
  - Sequence A single scan
  - Sequence A continuous scanning
  - Double sequence scanning, sequence A and B independently select trigger source, sequence B has higher priority than A
  - Synchronous mode (applicable to devices with two or three ADCs)
- Interrupt and Event Signal Output
  - Sequence A scan end interrupt EOCA_INT and event EOCA_EVENT
  - Sequence B scan end interrupt EOCB_INT and event EOCB_EVENT
  - Analog watchdog channel comparison interrupt CHCMP_INT and event CHCMP_EVENT, sequence comparison interrupt SEQCMP_INT and event SEQCMP_EVENT
  - The above 4 events can start DMA

1.4.17 Temperature sensor (OTS)

OTS can obtain the temperature inside the chip to support the reliable operation of the system. After using software or hardware to trigger the temperature measurement, OTS provides a set of temperature-related digital quantities, and the temperature value can be calculated through the calculation formula.

1.4.18 Advanced control timer (Timer6)

Advanced Control Timer 6 (Timer6) is a high-performance timer with a 16-bit count width, which can be used to count to generate different forms of clock waveforms and output for external use. The timer supports two waveform modes: triangle wave and sawtooth wave, and can generate various PWM waveforms; software synchronous counting and hardware synchronous counting can be realized between units; each reference value register supports buffering function; supports 2-phase quadrature encoding and 3-phase positive Cross code;

supports EMB control. This series of products is equipped with a 3-unit Timer6.

1.4.19 General control timer (Timer4)

General control timer 4 (Timer4) is a timer module for three-phase motor control. It provides three-phase motor control schemes for various applications. The timer supports triangular wave and sawtooth wave modes and generates various PWM waveforms. Supporting cache function; Support EMB control. 3 unit of Timer 4 is carried in this product family.

1.4.20 Emergency Brake Module (EMB)

The Emergency Brake Module is a functional module that notifies the timer to stop the output of PWM signals to the external motor when certain conditions are met. The following events are used to generate notifications:

- Change of input level of external port
- Level of PWM output port occurs in phase (same high or same low)
- Voltage comparator comparison results
- External oscillator stop oscillation
- Write register software control

1.4.21 General Timer (TimerA)

General Timer A (Timer A) is a timer with 16-bit count width and 4 PWM outputs. The timer supports two waveform modes: triangle wave and sawtooth wave, and can generate various PWM waveforms; supports software synchronization to start counting; comparison reference value register supports buffer function; supports 2-phase quadrature encoding counting and 3-phase quadrature encoding counting. This series of products are equipped with 6 units of TimerA, which can achieve a maximum of 48 PWM outputs.

1.4.22 General Timer (Timer0)

General timer 0 (Timer0) is a basic timer that can realize synchronous counting and asynchronous counting. The timer contains 2 channels, which can generate a compare match event during the counting period. The event can trigger interrupt, or can be output as an event

to control other modules. This series of products is equipped with 2 units of Timer0.

1.4.23 Real Time Clock (RTC)

Real Time Clock (RTC) is a counter that saves time information in BCD format. Record the specific calendar time from year 00 to year 99. Support 12/24 hour two time system, automatically calculate the number of days 28, 29 (leap year), 30 and 31 according to the month and year.

1.4.24 Watchdog counter (WDT)

There are two watchdog counters. One is a dedicated watchdog counter (SWDT) whose counting clock source is a dedicated internal RC (WDTCLK: 10KHz), and the other is a general-purpose watchdog counter (WDT) whose counting clock source is PCLK3.). The dedicated watchdog and general watchdog are 16-bit down counters used to monitor software failures caused by external interference or unforeseen logic conditions that cause the application to deviate from normal operation.

Both watchdogs support window functions. The window interval can be preset before the counting starts. When the count value is in the window interval, the counter can be refreshed and the counting restarts.

1.4.25 Serial Communication Interface (USART)

This product is equipped with 4 units of serial communication interface module (USART). The serial communication interface module (USART) can flexibly exchange full-duplex data with external devices; this USART supports universal asynchronous serial communication interface (UART), clock synchronous communication interface, and smart card interface (ISO/IEC7816-3). Support modem operation (CTS/RTS operation), multi-processor operation.

1.4.26 Inter-integrated circuit bus (I2C)

This product is equipped with 3 units of integrated circuit bus (I2C). I2C is used as the interface between the microcontroller and the I2C serial bus. Provide multi-master mode

function, can control all I2C bus protocol, arbitration. Support standard mode, fast mode.

1.4.27 Serial Peripheral Interface (SPI)

SPI is equipped with six channel serial peripheral interface, which supports high-speed full-duplex serial synchronous transmission and convenient data exchange with peripheral equipment. Users can set the range of 3/4-wire, host/slave and baud rate as needed.

1.4.28 Four-wire serial peripheral interface (QSPI)

The four-wire serial peripheral interface (QSPI) is a memory control module, which is mainly used to communicate with a serial ROM with an SPI compatible interface. Its objects mainly include serial flash memory, serial EEPROM and serial FeRAM.

1.4.29 Integrated circuit built-in audio bus (I2S)

I2S (Inter_IC Sound Bus), integrated circuit built-in audio bus, this bus is dedicated to data transmission between audio devices. This product is equipped with 4 I2S and has the following characteristics.

Function	Main characteristics
Communication mode	• Support full-duplex and half-duplex communication • Support host mode or slave mode operation
Data format	• Optional channel length: 16/32 bits • Optional transmission data length: 16/24/32bits • Data shift sequence: MSB starts
Baud rate	• 8-bit programmable linear prescaler for accurate audio sampling frequency • Support sampling frequency 192k, 96k, 48k, 44.1k, 32k, 22.05k, 16k, 8k • Can output drive clock to drive external audio components, the ratio is fixed at 256*Fs (Fs is the audio sampling frequency)
Support I2S protocol	• I2S Philips standard • MSB alignment standard • LSB alignment standard • PCM standard
Data buffer	• With 2-word deep, 32-bit wide input and output FIFO buffer area
Timer	• Internal I2SCLK (UPLLR/UPLLQ/UPLLP/MPLLR/MPLLQ/MPLLP) can be used; it can also be provided by an external clock on the I2S_EXCK pin

Interrupt	• An interrupt is generated when the effective space of the send buffer reaches the alarm threshold • An interrupt is generated when the effective space of the receive buffer reaches the alarm threshold • The receive data area is full and there are still write data requests, and receive overflow • The sending data area is empty and there are still sending requests, sending underflow • Send data area is full and still have write data request, send overflow

1.4.30 CAN communication interface (CAN)

This product is equipped with a CAN communication interface module (CAN), and is equipped with 512Byte RAM for CAN to store sending/receiving messages. It supports the CAN2.0B protocol specified by ISO11898-1 and the TTCAN protocol specified by ISO11898-4.

1.4.31 USB2.0 full speed module (USB FS)

This product is equipped with 1 unit of USB2.0 full-speed module (USB FS), built-in full-speed PHY on chip. USB FS is a dual-role (DRD) controller that supports both slave and host functions. In master mode, USB FS supports full-speed and low-speed transceivers, while in slave mode only full-speed transceivers are supported.

The USB FS module equipped with this product can generate an SOF event when the SOF token is successfully sent in the master mode or the SOF token is successfully received in the slave mode.

1.4.32 Encryption Co-Processing Module (CPM)

The encryption co-processing module (CPM) includes three sub-modules: AES encryption and decryption algorithm processor, HASH secure hash algorithm, and TRNG true random number generator.

The AES encryption and decryption algorithm processor follows the standard data encryption and decryption standards, and can realize encryption and decryption operations with a 128-bit key length.

The HASH secure hash algorithm is the SHA-2 version of SHA-256 (Secure Hash Algorithm), which complies with the national standard "FIPS PUB 180-3" issued by the National Bureau

of Standards and Technology of the United States. It can handle messages up to 2^64 bits in length. Produce 256-bit message digest output.

TRNG true random number generator is a random number generator based on continuous analog noise, providing 64bit random numbers.

1.4.33 Data Calculation Unit (DCU)

The Data Computing Unit is a module that simply processes data without relying on the CPU. Each DCU unit has 3 data registers, capable of adding, subtracting, and comparing the size of 2 data, as well as the window comparison function. This product is equipped 4 DCU units, each unit can perform its own function independently.

1.4.34 CRC Unit (CRC)

The CRC algorithm of this module complies with the definition of ISO/IEC 13239 and adopts 32-bit and 16-bit CRC respectively. The generator polynomial of CRC32 is $X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^{8}+X^{7}+X^{5}+X^{4}+X^{2}+X+1$. The generator polynomial of CRC16 is $X^{16}+X^{12}+X^{5}+1$.

1.4.35 SDIO Controller (SDIOC)

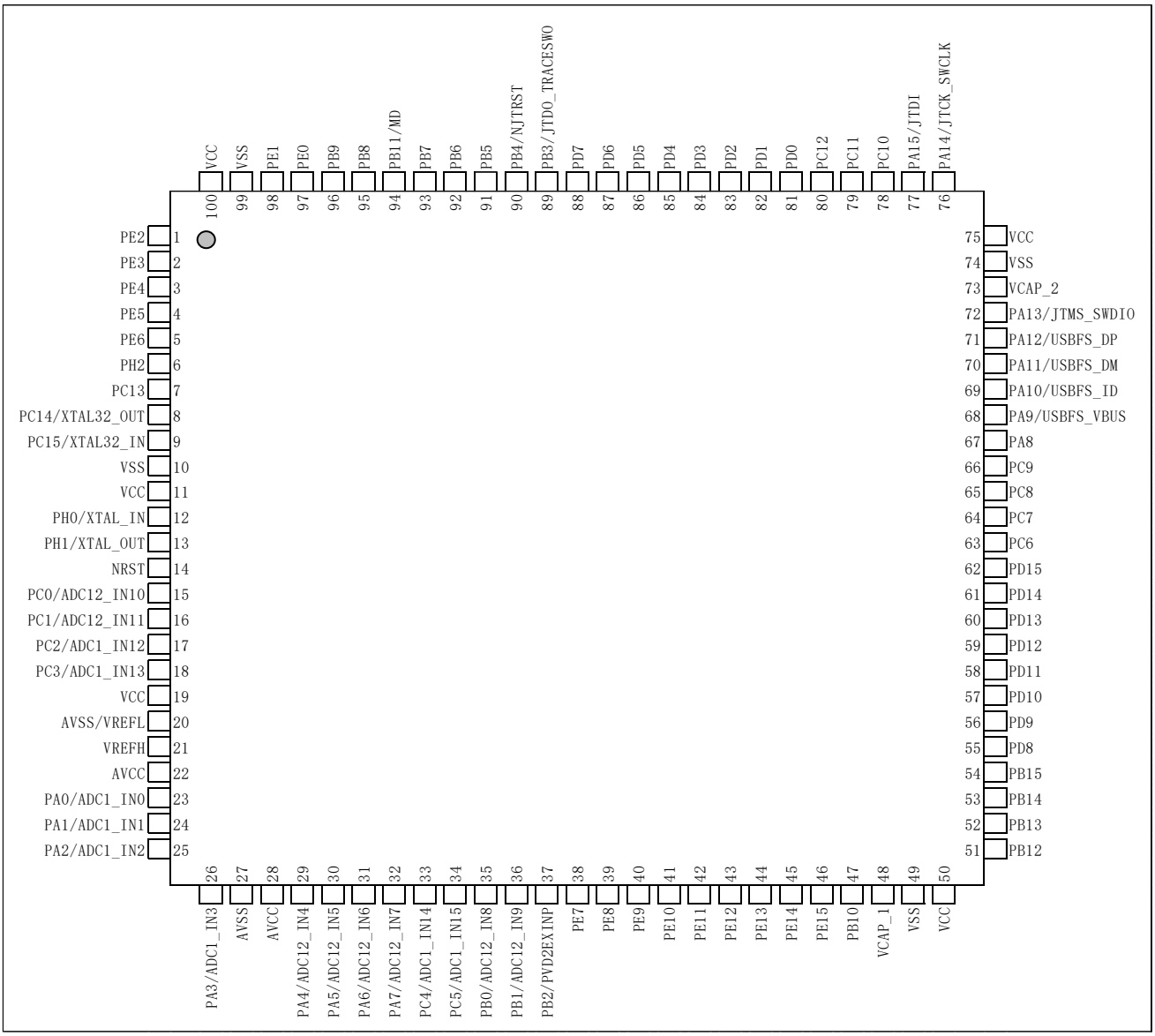
The SDIO controller is the host in the SD/SDIO/MMC communication protocol. This product has 2 SDIO controllers. Each SDIO controller provides a host interface for communicating with SD cards that support SD2.0 protocol, SDIO devices, and MMC devices that support eMMC4.51 protocol. The features of SDIOC are as follows:

- Support SDSC, SDHC, SDXC format SD cards and SDIO devices
- Support one-wire (1bit) and four-wire (4bit) SD bus
- Support one-wire (1bit), four-wire (4bit) and eight-wire (8bit) MMC bus
- With card recognition and hardware write protection function

2 Pin Configuration and Functions (Pinouts)

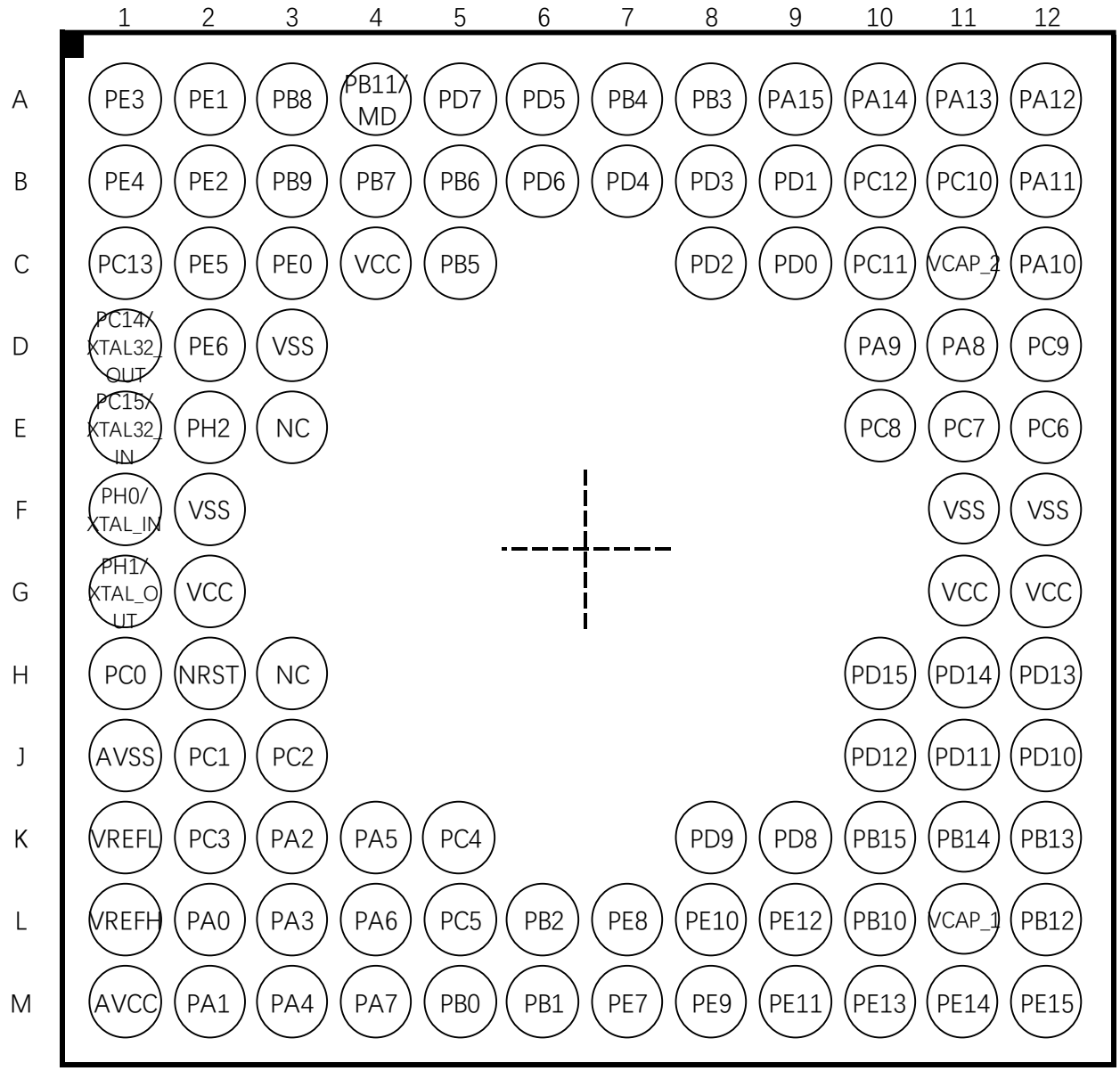
2.1 Pin configuration diagram

HC32F460PETB-LQFP100 /HC32F460PCTB-LQFP100



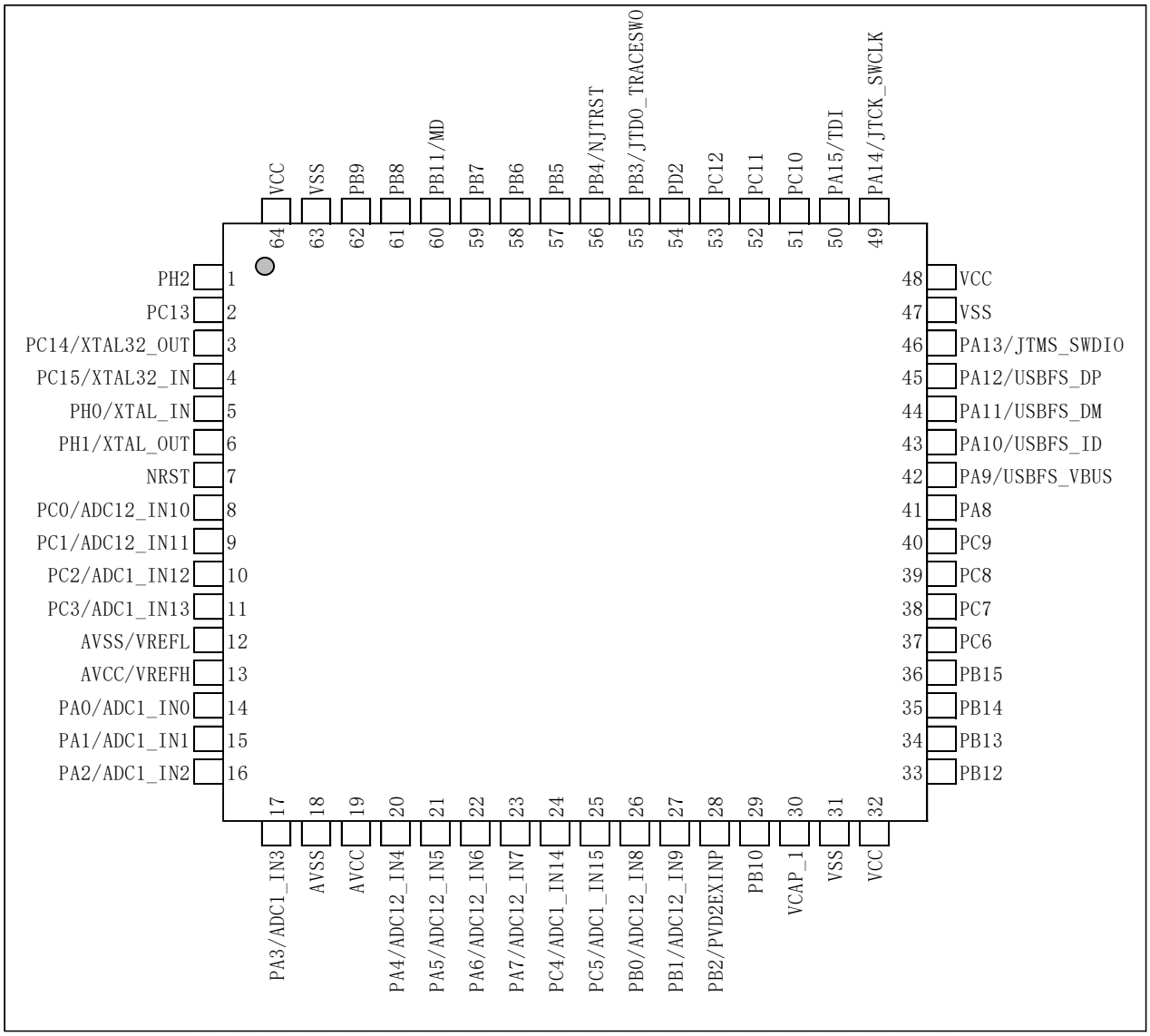
HC32F460PEHB-VFBGA100

(Top View)

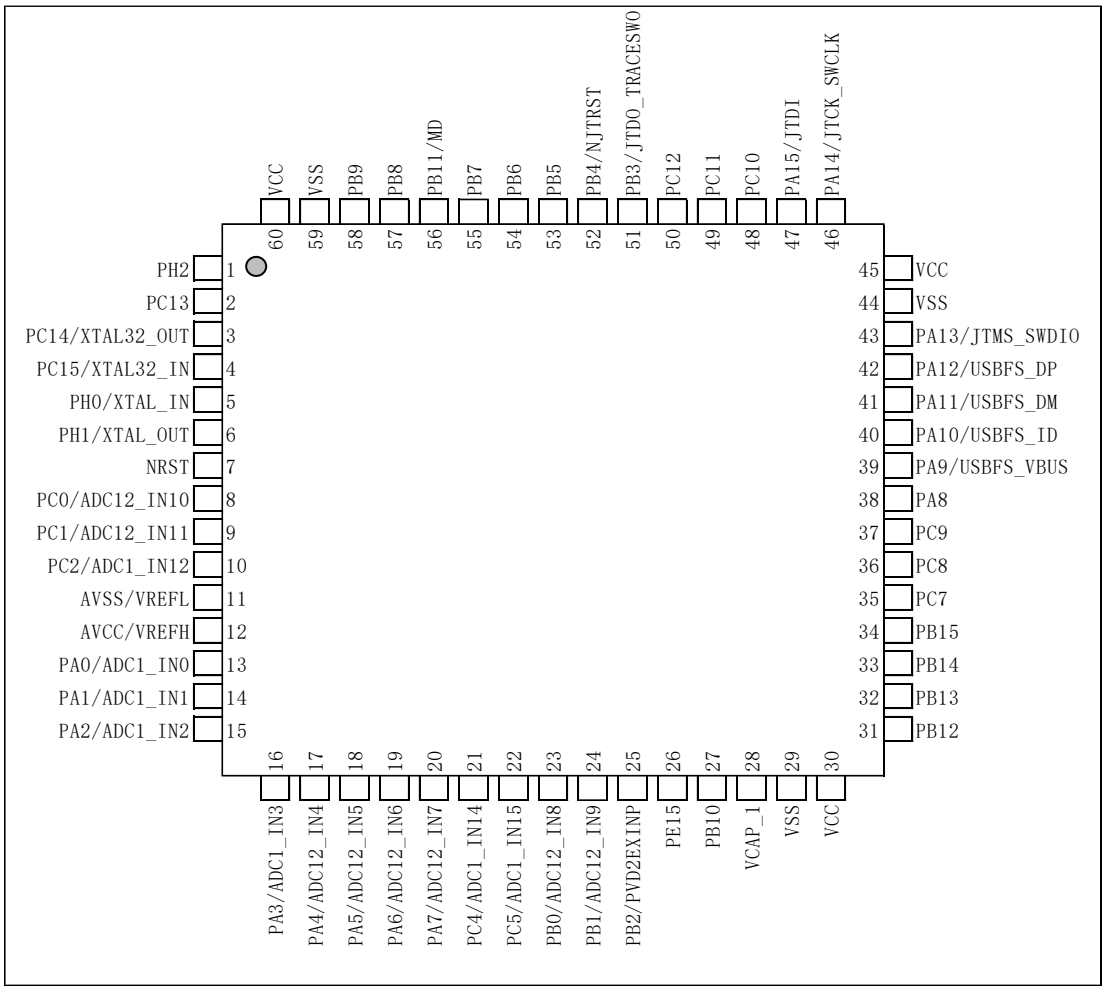


Note: A1 is Pin 1.

HC32F460KETA-LQFP64/ HC32F460KCTA-LQFP64



HC32F460KEUA-QFN60TR



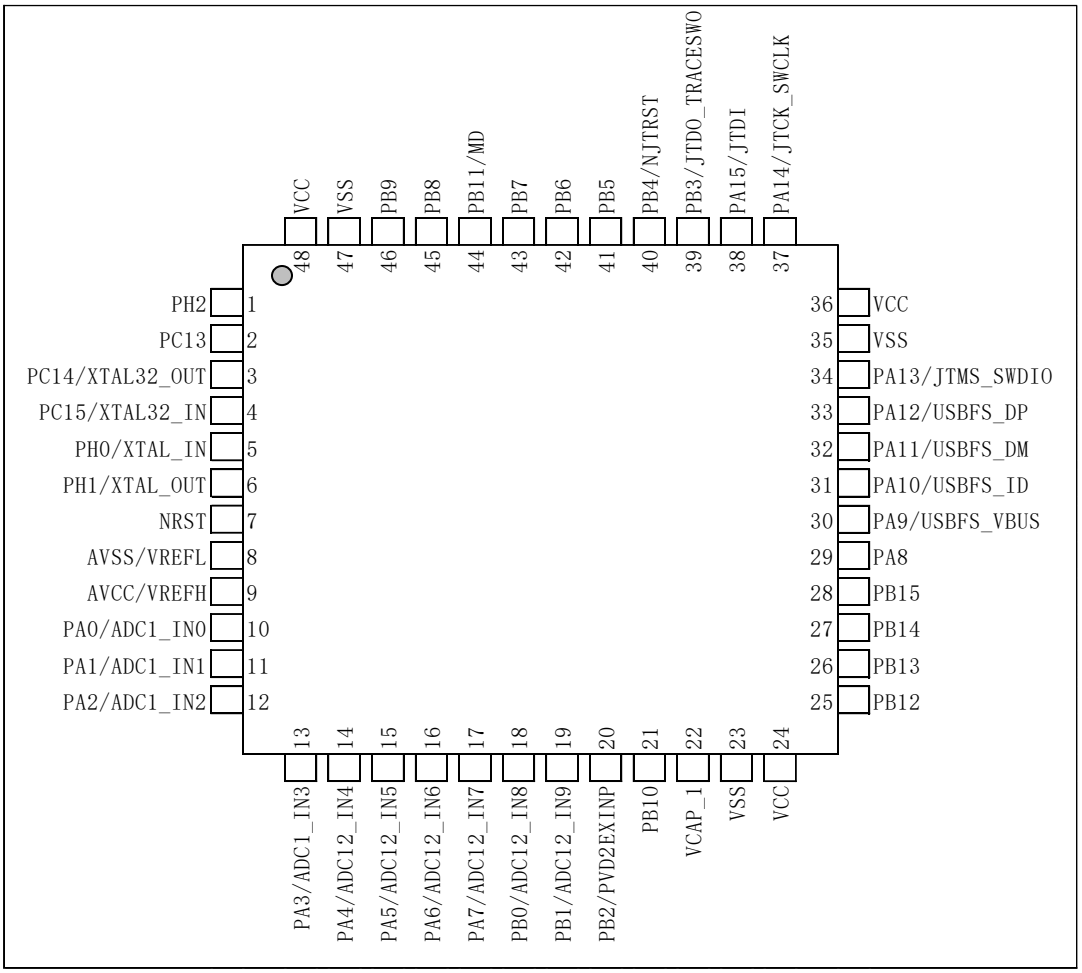


Figure 2 - 1 Pin configuration diagram

2.2 Pin function table

LQFP 100	VFBGA100	LQFP 64	QFN60	LQFP/QFN48	Pin Name	Analog	EIRQ/WKUP	TRACE/JTAG/SWD	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15	Func16~31	Func32~63
									GPO	other	TIM4	TIM6	TIMA	TIMA	EMB, TIMA	USART/SPI/QSPI	KEY	SDIO	USBFS/I2S	-	-	-	EVNTPT	EVENTOUT	-	Communication Funcs
1	B2	-	-	-	PE2		EIRQ2	TRACECK	GPO				TIMA_3_PWM5			USART3_CK								EVENTOUT		Func_Grp2
2	A1	-	-	-	PE3		EIRQ3	TRACED0	GPO				TIMA_3_PWM6			USART4_CK								EVENTOUT		Func_Grp2
3	B1	-	-	-	PE4		EIRQ4	TRACED1	GPO				TIMA_3_PWM7											EVENTOUT		Func_Grp2
4	C2	-	-	-	PE5		EIRQ5	TRACED2	GPO				TIMA_3_PWM8											EVENTOUT		Func_Grp2
5	D2	-	-	-	PE6		EIRQ6	TRACED3	GPO															EVENTOUT		Func_Grp2
6	E2	1	1	1	PH2		EIRQ2		GPO	FCMREF	TIM4_2_CLK		TIMA_4_PWM7		EMB_IN4			SDIO2_D4	I2S3_EXCK					EVENTOUT		Func_Grp2
7	C1	2	2	2	PC13		EIRQ13		GPO	RTC_OUT			TIMA_4_PWM8					SDIO2_CK	I2S3_MCK				EVNTP313			Func_Grp2
8	D1	3	3	3	PC14	XTAL32_OUT	EIRQ14		GPO				TIMA_4_PWM5										EVNTP314			
9	E1	4	4	4	PC15	XTAL32_IN	EIRQ15		GPO				TIMA_4_PWM6										EVNTP315			
10	F2	-	-	-	VSS																					
11	G2	-	-	-	VCC																					
12	F1	5	5	5	PH0	XTAL_IN	EIRQ0		GPO					TIMA_5_PWM3												
13	G1	6	6	6	PH1	XTAL_OUT	EIRQ1		GPO					TIMA_5_PWM4												
14	H2	7	7	7	NRST																					
15	H1	8	8	-	PC0	ADC12_IN10/CMP3_INP3	EIRQ0		GPO				TIMA_2_PWM5					SDIO2_D5					EVNTP300	EVENTOUT		Func_Grp1
16	J2	9	9	-	PC1	ADC12_IN11	EIRQ1		GPO				TIMA_2_PWM6					SDIO2_D6					EVNTP301	EVENTOUT		Func_Grp1
17	J3	10	10	-	PC2	ADC1_IN12	EIRQ2		GPO				TIMA_2_PWM7		EMB_IN3			SDIO2_D7					EVNTP302	EVENTOUT		Func_Grp1
18	K2	11	-	-	PC3	ADC1_IN13/CMP1_INM2	EIRQ3		GPO				TIMA_2_PWM8					SDIO1_WP					EVNTP303	EVENTOUT		Func_Grp1
19	-	-	-	-	VCC																					
20	J1	12	11	8	AVSS																					
-	K1	-	-	-	VREFL																					
21	L1	-	-	-	VREFH																					
22	M1	13	12	9	AVCC																					
23	L2	14	13	10	PA0	ADC1_IN0/CMP1_INP1	EIRQ0/WKUP0_0		GPO		TIM4_2_OUH		TIMA_2_PWM1/TIMA_2_CLKA		TIMA_2_TRIG	SPI1_SS1		SDIO2_D4					EVNTP100	EVENTOUT		Func_Grp1

LQFP 100	VFBGA100	LQFP 64	QFN60	LQFP/QFN48	Pin Name	Analog	EIRQ/WKUP	TRACE/JTAG/SWD	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15	Func16~31	Func32~63
									GPO	other	TIM4	TIM6	TIMA	TIMA	EMB, TIMA	USART/SPI/QSPI	KEY	SDIO	USBFS/I2S	-	-	-	EVNTPT	EVENTOUT	-	Communication Funcs
24	M2	15	14	11	PA1	ADC1_IN1/CMP1_INP2	EIRQ1		GPO		TIM4_2_OUL		TIMA_2_PWM2/TIMA_2_CLKB	TIMA_3_TRIG		SPI1_SS2		SDIO2_D5					EVNTP101	EVENTOUT		Func_Grp1
25	K3	16	15	12	PA2	ADC1_IN2/CMP1_INP3	EIRQ2		GPO		TIM4_2_OVH		TIMA_2_PWM3	TIMA_5_PWM1/TIMA_5_CLKA		SPI1_SS3		SDIO2_D6					EVNTP102	EVENTOUT		Func_Grp1
26	L3	17	16	13	PA3	ADC1_IN3/PGAVSS/CMP1_INP4	EIRQ3		GPO		TIM4_2_OVL		TIMA_2_PWM4	TIMA_5_PWM2/TIMA_5_CLKB				SDIO2_D7					EVNTP103	EVENTOUT		Func_Grp1
27	-	18	-	-	AVSS																					
-	E3	-	-	-	NC																					
28	-	19	-	-	AVCC																					
29	M3	20	17	14	PA4	ADC12_IN4/CMP2_INP1/CMP3_INP4	EIRQ4		GPO		TIM4_2_OWH			TIMA_3_PWM5		USART2_CK	KEYOUT0		I2S1_EXCK				EVNTP104	EVENTOUT		Func_Grp1
30	K4	21	18	15	PA5	ADC12_IN5/CMP2_INP2	EIRQ5		GPO		TIM4_2_OWL		TIMA_2_PWM1/TIMA_2_CLKA	TIMA_3_PWM6	TIMA_2_TRIG		KEYOUT1		I2S1_MCK				EVNTP105	EVENTOUT		Func_Grp1
31	L4	22	19	16	PA6	ADC12_IN6/CMP2_INP3	EIRQ6		GPO					TIMA_3_PWM1/TIMA_3_CLKA	EMB_IN2		KEYOUT2	SDIO1_CMD					EVNTP106	EVENTOUT		Func_Grp1
32	M4	23	20	17	PA7	ADC12_IN7/CMP1_INM1/CMP2_INM1/CMP3_INM1	EIRQ7		GPO		TIM4_1_OUL	TIM6_1_PWMB	TIMA_1_PWM5	TIMA_3_PWM2/TIMA_3_CLKB	EMB_IN3		KEYOUT3	SDIO2_WP					EVNTP107	EVENTOUT		Func_Grp1
33	K5	24	21	-	PC4	ADC1_IN14/CMP2_INM2	EIRQ4		GPO		TIM4_2_OUH			TIMA_3_PWM7		USART1_CK		SDIO2_CD					EVNTP304	EVENTOUT		Func_Grp1
34	L5	25	22	-	PC5	ADC1_IN15/CMP3_INM2	EIRQ5		GPO		TIM4_2_OUL			TIMA_3_PWM8				SDIO2_CMD					EVNTP305	EVENTOUT		Func_Grp1
35	M5	26	23	18	PB0	ADC12_IN8/CMP3_INP1	EIRQ0		GPO		TIM4_1_OVL	TIM6_2_PWMB	TIMA_1_PWM6	TIMA_3_PWM3		USART4_CK	KEYOUT4	SDIO2_CMD					EVNTP200	EVENTOUT		Func_Grp1
36	M6	27	24	19	PB1	ADC12_IN9/CMP3_INP2	EIRQ1/WKUP0_1		GPO		TIM4_1_OWL	TIM6_3_PWMB	TIMA_1_PWM7	TIMA_3_PWM4		QSPI_QSSN	KEYOUT5	SDIO2_D3	I2S2_EXCK				EVNTP201	EVENTOUT		Func_Grp1
37	L6	28	25	20	PB2	PVD2EXINP	EIRQ2/WKUP0_2		GPO	VCOUT123		TIM6_TRIGB	TIMA_1_PWM8		EMB_IN1	QSPI_QSIO3		SDIO2_D2	I2S2_MCK				EVNTP202	EVENTOUT		Func_Grp1
38	M7	-	-	-	PE7		EIRQ7		GPO	ADTRG1		TIM6_TRIGA	TIMA_1_TRIG			USART1_CK								EVENTOUT		
39	L7	-	-	-	PE8		EIRQ8		GPO		TIM4_1_OUL	TIM6_1_PWMB	TIMA_1_PWM5											EVENTOUT		
40	M8	-	-	-	PE9		EIRQ9		GPO		TIM4_1_OUH	TIM6_1_PWMA	TIMA_1_PWM1/TIMA_1_CLKA											EVENTOUT		
41	L8	-	-	-	PE10		EIRQ10		GPO		TIM4_1_OVL	TIM6_2_PWMB	TIMA_1_PWM6											EVENTOUT		

LQFP 100	VFBGA100	LQFP 64	QFN60	LQFP/QFN48	Pin Name	Analog	EIRQ/WKUP	TRACE/JTAG/SWD	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15	Func16~31	Func32~63
									GPO	other	TIM4	TIM6	TIMA	TIMA	EMB, TIMA	USART/SPI/QSPI	KEY	SDIO	USBFS/I2S	-	-	-	EVNTPT	EVENTOUT	-	Communication Funcs
42	M9	-	-	-	PE11		EIRQ11		GPO		TIM4_1_OVH	TIM6_2_PWMA	TIMA_1_PWM2/TIMA_1_CLKB											EVENTOUT		
43	L9	-	-	-	PE12		EIRQ12		GPO		TIM4_1_OWL	TIM6_3_PWMB	TIMA_1_PWM7			SPI1_SS1								EVENTOUT		Func_Grp2
44	M10	-	-	-	PE13		EIRQ13		GPO		TIM4_1_OWH	TIM6_3_PWMA	TIMA_1_PWM3			SPI1_SS2								EVENTOUT		Func_Grp2
45	M11	-	-	-	PE14		EIRQ14		GPO		TIM4_1_CLK		TIMA_1_PWM4			SPI1_SS3		SDIO1_CD						EVENTOUT		Func_Grp2
46	M12	-	26	-	PE15		EIRQ15		GPO				TIMA_1_PWM8	TIMA_5_TRIG	EMB_IN2	USART4_CK		SDIO1_WP						EVENTOUT		Func_Grp2
47	L10	29	27	21	PB10		EIRQ10		GPO	ADTRG2	TIM4_2_OVH		TIMA_2_PWM3	TIMA_5_PWM8		QSPI_QSIO2		SDIO1_D7	I2S3_EXCK				EVNTP210	EVENTOUT		Func_Grp2
48	L11	30	28	22	VCAP_1																					
49	F12	31	29	23	VSS																					
50	G12	32	30	24	VCC																					
51	L12	33	31	25	PB12		EIRQ12		GPO	VCOUT1	TIM4_2_OVL	TIM6_TRIGB	TIMA_1_PWM8		EMB_IN2	QSPI_QSIO1		SDIO2_D1	I2S3_MCK				EVNTP212	EVENTOUT		Func_Grp2
52	K12	34	32	26	PB13		EIRQ13		GPO	VCOUT2	TIM4_1_OUL	TIM6_1_PWMB	TIMA_1_PWM5			QSPI_QSIO0		SDIO2_D0					EVNTP213	EVENTOUT		Func_Grp2
53	K11	35	33	27	PB14		EIRQ14		GPO	VCOUT3	TIM4_1_OVL	TIM6_2_PWMB	TIMA_1_PWM6			QSPI_QSCK		SDIO1_D6					EVNTP214	EVENTOUT		Func_Grp2
54	K10	36	34	28	PB15		EIRQ15		GPO	RTC_OUT	TIM4_1_OWL	TIM6_3_PWMB	TIMA_1_PWM7	TIMA_6_TRIG	EMB_IN4	USART3_CK		SDIO1_CK					EVNTP215	EVENTOUT		Func_Grp2
55	K9	-	-	-	PD8		EIRQ8		GPO		TIM4_3_OUL			TIMA_6_PWM1/TIMA_6_CLKA		QSPI_QSIO0	KEYOUT7						EVNTP408	EVENTOUT		Func_Grp2
56	K8	-	-	-	PD9		EIRQ9		GPO		TIM4_3_OVL			TIMA_6_PWM2/TIMA_6_CLKB		QSPI_QSIO1	KEYOUT6						EVNTP409	EVENTOUT		Func_Grp2
57	J12	-	-	-	PD10		EIRQ10		GPO		TIM4_3_OWL			TIMA_6_PWM3		QSPI_QSIO2	KEYOUT5						EVNTP410	EVENTOUT		Func_Grp2
58	J11	-	-	-	PD11		EIRQ11		GPO		TIM4_3_CLK			TIMA_6_PWM4		QSPI_QSIO3	KEYOUT4						EVNTP411	EVENTOUT		Func_Grp2
59	J10	-	-	-	PD12		EIRQ12		GPO				TIMA_4_PWM1/TIMA_4_CLKA	TIMA_5_PWM5									EVNTP412	EVENTOUT		
60	H12	-	-	-	PD13		EIRQ13		GPO				TIMA_4_PWM2/TIMA_4_CLKB	TIMA_5_PWM6									EVNTP413	EVENTOUT		
61	H11	-	-	-	PD14		EIRQ14		GPO				TIMA_4_PWM3	TIMA_5_PWM7									EVNTP414	EVENTOUT		
62	H10	-	-	-	PD15		EIRQ15		GPO				TIMA_4_PWM4	TIMA_5_PWM8									EVNTP415	EVENTOUT		
63	E12	37	-	-	PC6		EIRQ6		GPO				TIMA_3_PWM1/TIMA_3_CLKA	TIMA_5_PWM8		QSPI_QSCK	KEYOUT3	SDIO1_D6					EVNTP306	EVENTOUT		Func_Grp2
64	E11	38	35	-	PC7		EIRQ7		GPO		TIM4_2_CLK		TIMA_3_PWM2/TIMA_3_CLKB	TIMA_5_PWM7		QSPI_QSSN	KEYOUT2	SDIO1_D7	I2S2_EXCK				EVNTP307	EVENTOUT		Func_Grp2

LQFP 100	VFBGA100	LQFP 64	QFN60	LQFP/QFN48	Pin Name	Analog	EIRQ/WKUP	TRACE/JTAG/SWD	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15	Func16~31	Func32~63
									GPO	other	TIM4	TIM6	TIMA	TIMA	EMB, TIMA	USART/SPI/QSPI	KEY	SDIO	USBFS/I2S	-	-	-	EVNTPT	EVENTOUT	-	Communication Funcs
65	E10	39	36	-	PC8		EIRQ8		GPO		TIM4_2_OWH		TIMA_3_PWM3	TIMA_5_PWM6		USART3_CK	KEYOUT1	SDIO1_D0	I2S2_MCK				EVNTP308	EVENTOUT		Func_Grp2
66	D12	40	37	-	PC9		EIRQ9		GPO	MCO_2	TIM4_2_OWL		TIMA_3_PWM4	TIMA_5_PWM5			KEYOUT0	SDIO1_D1					EVNTP309	EVENTOUT		Func_Grp1
67	D11	41	38	29	PA8		EIRQ8/WKUP2_0		GPO	MCO_1	TIM4_1_OUH	TIM6_1_PWMA	TIMA_1_PWM1/TIMA_1_CLKA			USART1_CK		SDIO1_D1	USBFS_SOF				EVNTP108	EVENTOUT		Func_Grp1
68	D10	42	39	30	PA9		EIRQ9/WKUP2_1		GPO		TIM4_1_OVH	TIM6_2_PWMA	TIMA_1_PWM2/TIMA_1_CLKB					SDIO1_D2	USBFS_VBUS				EVNTP109	EVENTOUT		Func_Grp1
69	C12	43	40	31	PA10		EIRQ10/WKUP2_2		GPO		TIM4_1_OWH	TIM6_3_PWMA	TIMA_1_PWM3	TIMA_5_TRIG				SDIO1_CD	USBFS_ID				EVNTP110	EVENTOUT		Func_Grp1
70	B12	44	41	32	PA11		EIRQ11/WKUP2_3		GPO		TIM4_1_CLK		TIMA_1_PWM4		EMB_IN1			SDIO2_CD	USBFS_DM				EVNTP111	EVENTOUT		Func_Grp1
71	A12	45	42	33	PA12		EIRQ12/WKUP3_0		GPO		TIM4_3_OWL	TIM6_TRIGA	TIMA_1_TRIG	TIMA_6_PWM1/TIMA_6_CLKA				SDIO2_WP	USBFS_DP				EVNTP112	EVENTOUT		Func_Grp1
72	A11	46	43	34	PA13		EIRQ13/WKUP3_1	JTMS_SWDIO	GPO				TIMA_2_PWM5	TIMA_6_PWM2/TIMA_6_CLKB		SPI2_SS1		SDIO2_D3					EVNTP113	EVENTOUT		Func_Grp1
73	C11	-	-	-	VCAP_2																					
74	F11	47	44	35	VSS																					
75	G11	48	45	36	VCC																					
76	A10	49	46	37	PA14		EIRQ14/WKUP3_2	JTCK_SWCLK	GPO				TIMA_2_PWM6	TIMA_6_PWM3	TIMA_4_TRIG	SPI2_SS2		SDIO2_D2	I2S1_EXCK				EVNTP114	EVENTOUT		Func_Grp1
77	A9	50	47	38	PA15		EIRQ15/WKUP3_3	JTDI	GPO				TIMA_2_PWM1/TIMA_2_CLKA	TIMA_6_PWM4	TIMA_2_TRIG	SPI2_SS3		SDIO2_D1	I2S1_MCK				EVNTP115	EVENTOUT		Func_Grp1
78	B11	51	48	-	PC10		EIRQ10		GPO		TIM4_3_OUH		TIMA_2_PWM7	TIMA_5_PWM1/TIMA_5_CLKA				SDIO1_D2					EVNTP310	EVENTOUT		Func_Grp1
79	C10	52	49	-	PC11		EIRQ11		GPO		TIM4_3_OVH		TIMA_2_PWM8	TIMA_5_PWM2/TIMA_5_CLKB				SDIO1_D3					EVNTP311	EVENTOUT		Func_Grp1
80	B10	53	50	-	PC12		EIRQ12		GPO		TIM4_3_OWH		TIMA_4_TRIG	TIMA_5_PWM3				SDIO1_CK					EVNTP312	EVENTOUT		Func_Grp1
81	C9	-	-	-	PD0		EIRQ0		GPO	VCOUT123				TIMA_5_PWM4									EVNTP400	EVENTOUT		Func_Grp1
82	B9	-	-	-	PD1		EIRQ1		GPO				TIMA_3_TRIG	TIMA_6_PWM5									EVNTP401	EVENTOUT		Func_Grp1
83	C8	54	-	-	PD2		EIRQ2		GPO				TIMA_2_PWM4	TIMA_6_PWM6				SDIO1_CMD					EVNTP402	EVENTOUT		Func_Grp1
84	B8	-	-	-	PD3		EIRQ3		GPO	VCOUT1				TIMA_6_PWM7									EVNTP403	EVENTOUT		
85	B7	-	-	-	PD4		EIRQ4		GPO	VCOUT2				TIMA_6_PWM8									EVNTP404	EVENTOUT		
86	A6	-	-	-	PD5		EIRQ5		GPO	VCOUT3													EVNTP405	EVENTOUT		
87	B6	-	-	-	PD6		EIRQ6		GPO							USART2_CK							EVNTP406	EVENTOUT		
88	A5	-	-	-	PD7		EIRQ7		GPO							USART2_CK							EVNTP407	EVENTOUT		

LQFP 100	VFBGA100	LQFP 64	QFN60	LQFP/QFN48	Pin Name	Analog	EIRQ/WKUP	TRACE/JTAG/SWD	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15	Func16~31	Func32~63
									GPO	other	TIM4	TIM6	TIMA	TIMA	EMB, TIMA	USART/SPI/QSPI	KEY	SDIO	USBFS/I2S	-	-	-	EVNTPT	EVENTOUT	-	Communication Funcs
89	A8	55	51	39	PB3		EIRQ3/WKUP0_3	JTDO_TRACESWO	GPO	FCMREF	TIM4_3_CLK		TIMA_2_PWM2/TIMA_2_CLKB	TIMA_6_PWM5				SDIO2_D0					EVNTP203	EVENTOUT		Func_Grp2
90	A7	56	52	40	PB4		EIRQ4/WKUP1_0	NJTRST	GPO		TIM4_3_OWL		TIMA_3_PWM1/TIMA_3_CLKA	TIMA_6_PWM6				SDIO1_D0					EVNTP204	EVENTOUT		Func_Grp2
91	C5	57	53	41	PB5		EIRQ5/WKUP1_1		GPO		TIM4_3_OWH		TIMA_3_PWM2/TIMA_3_CLKB	TIMA_6_PWM7				SDIO1_D3	I2S4_EXCK				EVNTP205	EVENTOUT		Func_Grp2
92	B5	58	54	42	PB6		EIRQ6/WKUP1_2		GPO	ADTRG2	TIM4_3_OVL		TIMA_4_PWM1/TIMA_4_CLKA	TIMA_6_PWM8				SDIO2_CK	I2S4_MCK				EVNTP206	EVENTOUT		Func_Grp2
93	B4	59	55	43	PB7		EIRQ7/WKUP1_3		GPO	ADTRG1	TIM4_3_OVH		TIMA_4_PWM2/TIMA_4_CLKB					SDIO1_D0					EVNTP207	EVENTOUT		Func_Grp2
94	A4	60	56	44	PB11/MD		NMI																EVNTP211			
95	A3	61	57	45	PB8		EIRQ8		GPO		TIM4_3_OUL		TIMA_4_PWM3				KEYOUT7	SDIO1_D4	USBFS_DRVVBUS				EVNTP208	EVENTOUT		Func_Grp2
96	B3	62	58	46	PB9		EIRQ9		GPO		TIM4_3_OUH		TIMA_4_PWM4	TIMA_6_TRIG		SPI2_SS1	KEYOUT6	SDIO1_D5					EVNTP209	EVENTOUT		Func_Grp2
97	C3	-	-	-	PE0		EIRQ0		GPO	MCO_1			TIMA_4_TRIG			SPI2_SS2								EVENTOUT		Func_Grp2
98	A2	-	-	-	PE1		EIRQ1		GPO	MCO_2	TIM4_3_CLK					SPI2_SS3								EVENTOUT		Func_Grp2
99	D3	63	59	47	VSS																					
100	C4	64	60	48	VCC																					
-	H3	-	-	-	NC																					

Table2 - 1 Pin function table

Note:

– In the above table, there are 64 pins that support Func32~63 function selection. Func32~63 are mainly serial communication functions (including USART, SPI, I2C, I2S, CAN), divided into two groups Func_Grp1, Func_Grp2. For details, please refer toTable2-2 .

	Func32	Func33	Func34	Func35	Func36	Func37	Func38	Func39	Func40	Func41	Func42	Func43	Func44	Func45	Func46	Func47
Func_Grp 1	USART1_TX	USART1_RX	USART1_RTS	USART1_CTS	USART2_TX	USART2_RX	USART2_RTS	USART2_CTS	SPI1_MOSI	SPI1_MISO	SPI1_SS0	SPI1_SCK	SPI2_MOSI	SPI2_MISO	SPI2_SS0	SPI2_SCK
Func_Grp 2	USART3_TX	USART3_RX	USART3_RTS	USART3_CTS	USART4_TX	USART4_RX	USART4_RTS	USART4_CTS	SPI3_MOSI	SPI3_MISO	SPI3_SS0	SPI3_SCK	SPI4_MOSI	SPI4_MISO	SPI4_SS0	SPI4_SCK

	Func48	Func49	Func50	Func51	Func52	Func53	Func54	Func55	Func56	Func57	Func58	Func59	Func60	Func61	Func62	Func63
Func_Grp 1	I2C1_SDA	I2C1_SCL	I2C2_SDA	I2C2_SCL	I2S1_SD	I2S1_SDIN	I2S1_WS	I2S1_CK	I2S2_SD	I2S2_SDIN	I2S2_WS	I2S2_CK				
Func_Grp 2	I2C3_SDA	I2C3_SCL	CAN_TxD	CAN_RxD	I2S3_SD	I2S3_SDIN	I2S3_WS	I2S3_CK	I2S4_SD	I2S4_SDIN	I2S4_WS	I2S4_CK				

Table2-2 Func32~63 table

Package	Port Group	Bits																Pin Count	
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		Total
LQFP100	PortA	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	83
VFBGA100	PortB	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortC	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortD	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortE	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortH	-	-	-	-	-	-	-	-	-	-	-	-	-	o	o	o	3	
LQFP64	PortA	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	52
	PortB	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortC	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortD	-	-	-	-	-	-	-	-	-	-	-	-	-	o	-	-	1	
	PortH	-	-	-	-	-	-	-	-	-	-	-	-	-	o	o	o	3	
QFN60	PortA	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	50
	PortB	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortC	o	o	o	o	o	o	o	o	o	-	o	o	-	o	o	o	14	
	PortE	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	o	1	
	PortH	-	-	-	-	-	-	-	-	-	-	-	-	-	o	o	o	3	
LQFP48	PortA	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	38
QFN48	PortB	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortC	o	o	o	-	-	-	-	-	-	-	-	-	-	-	-	-	3	
	PortH	-	-	-	-	-	-	-	-	-	-	-	-	-	o	o	o	3	
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		

Table2-3 Port configuration

Port		Pull up	Open-drain output	Driving capacity	5V withstand voltage	Remark
PortA	PA0~PA10 PA13~PA15	Support	Support	Low Medium High	support*	
	PA11, PA12	Support	Support	Low Medium High	not support	
PortB	PB0~PB10, PB12~PB15	Support	Support	Low Medium High	support*	
	PB11	Support	-	-	Support	Input dedicated
PortC	PC0~PC15	Support	Support	Low Medium High	support*	
PortD	PD0~PD15	Support	Support	Low Medium High	Support	
PortE	PE0~PE15	Support	Support	Low Medium High	Support	
PortH	PH0~PH2	Support	Support	Low Medium High	Support	

Table2-4 General functional specifications

Note:

– When used as an analog function, the input voltage must not be higher than VREFH/AVCC.

2.3 Pin function description

Categories	Functional name	I/O	Note
Power	VCC	I	Power supply
	VSS	I	Source ground
	VCAP_1~2	IO	Core voltage
	AVCC	I	Analog power
	AVSS	I	Analog power ground
	VREFH	I	Analog reference voltage
	VREFL	I	Analog reference voltage
System	NRST	I	Reset pin, low effective.
	MD	I	Mode pin
PVD	PVD2EXINP	I	PVD2 external input comparison voltage
Clock	XTAL_IN	I	External master clock oscillator interface
	XTAL_OUT	O	
	XTAL32_IN	I	External sub clock (32K) oscillator interface
	XTAL32_OUT	O	
	MCO_1~2	O	Internal clock output
GPIO	GPIOxy (x= A~E,H, y=0~15)	IO	General input/output
EVENTOUT	EVENTOUT	O	Cortex-M4 CPU event output
EIRQ	EIRQx (x=0~15)	I	Shielded external interrupt
	WKUPx_y (x,y=0~3)	I	External wake-up input in PowerDown mode
	NMI	I	Non-shielded external interrupt
Event Port	EVNTPxy (x=1~4, y=0~15)	IO	Event port input and output function
Key	KEYOUTx(x=0~7)	O	KEYSCAN scan output signal
JTAG/SWD	JTCK_SWCLK	I	Online debugging interface
	JTMS_SWDIO	IO	
	JTDO_TRACESWO	O	
	JTDI	I	
	NJTRST	I	
TRACE	TRACECK	O	Tracking and debugging synchronous clock output
	TRACED0~3	O	Trace debugging data output
FCM	FCMREF	I	External reference clock input for clock frequency
RTC	RTCOUT	O	1Hz clock output
Timer4	TIM4_x_CLK	I	Counting clock port input

Categories	Functional name	I/O	Note
(x=1~3)	TIM4_x_OUH	IO	PWM port U-phase output
	TIM4_x_OUL	IO	PWM port U-phase output
	TIM4_x_OVH	IO	PWM port V-phase output
	TIM4_x_OVL	IO	PWM port V-phase output
	TIM4_x_OWH	IO	PWM port W-phase output
	TIM4_x_OWL	IO	PWM port W-phase output
Timer6	TIM6_TRIGA	I	External event triggers A input
(x=1~3)	TIM6_TRIGB	I	B input triggered by external event
	TIM6_x_PWMA	IO	External Event Trigger Input or PWM Port Output
	TIM6_x_PWMB	IO	External Event Trigger Input or PWM Port Output
TimerA	TIMA_x_TRIG	I	External event trigger input
(x=1~6)	TIMA_x_PWM1/TIMA_x_CLKA	IO	External event trigger input or PWM port output or count
	TIMA_x_PWM2/TIMA_x_CLKB	IO	External event trigger input or PWM port output or count
	TIMA_x_PWMy (y=3~8)	IO	External Event Trigger Input or PWM Port Output
EMB	EMB_INx (x=1~4)	I	Groupx (x=1~4) port input control signal
USARTx	USARTx_TX	IO	Send data
(x=1~4)	USARTx_RX	IO	Receiving data
	USARTx_CK	IO	Communication clock
	USARTx_RTS	O	Request to send a signal
	USARTx_CTS	I	Clear to send
SPIx	SPIx_MISO	IO	Primary input/secondary output data transfer pin
(x=1~4)	SPIx_MOSI	IO	Primary output/slave input data transfer pin
	SPIx_SCK	IO	Transmission clock
	SPIx_SS0	IO	Select input/output pin from machine
	SPIx_SS1~3	O	Slave select output pin
QSPI	QSPI_QSIO0~3	IO	Data line
	QSPI_QSCK	O	Clock output
	QSPI_QSSN	O	Slave selection
I2Cx	I2Cx_SCL	IO	Clock line
(x=1~3)	I2Cx_SDA	IO	Data line
I2Sx	I2Sx_SD	IO	Serial data
(x=1~4)	I2Sx_SDIN	I	Full duplex serial data input
	I2Sx_WS	IO	Word selection
	I2Sx_CK	IO	Serial clock

Categories	Functional name	I/O	Note
	I2Sx_EXCK	I	External timer
	I2Sx_MCK	O	Master clock
CAN	CAN_TxD	O	Send data
	CAN_RxD	I	Receiving data
SDIOx	SDIOx_Dy (y=0~7)	IO	SD data signal
	SDIOx_CK	O	SD clock output signal
	SDIOx_CMD	IO	SD command and reply signal
	SDIOx_CD	I	SD card recognition status signal
	SDIOx_WP	I	SD card write protection status signal
USBFS	USBFS_DM	IO	USBFS on-chip full-speed PHY D-signal
	USBFS_DP	IO	USBFS on-chip full-speed PHY D+ signal
	USBFS_VBUS	I	USBFS VBUS signal
	USBFS_ID	I	USBFS ID signal
	USBFS_SOF	O	USBFS SOF pulse output signal
	USBFS_DRVVBUS	O	USBFS VBUS drive permission signal
CMPx (x=1~3)	VCOUT1	O	Analog comparison channel 1 result output
	VCOUT2	O	Analog comparison channel 2 result output
	VCOUT3	O	Analog comparison channel 3 result output
	VCOUT123	O	Analog comparison channel 1~3 result OR output
	CMPx_INPy	I	Analog comparator channel x positive terminal voltage y
	CMPx_INMy	I	Analog comparator channel x negative terminal voltage y
ADC	ADTRG1	I	ADC1 AD conversion external start source
	ADTRG2	I	ADC2 AD conversion external start source
	ADC1_INx (x=0~3,12~15)	I	ADC1 external analog input port
	ADC12_INx (x=4~11)	I	ADC1 and ADC2 share external analog input port
	PGAVSS	I	PGA Ground input

Table2-5 Pin function description

2.4 Pin instruction

Pin name	Usage notes
VCC	Power supply, connect 1.8V~3.6V voltage, and connect decoupling capacitor to VSS pin nearby (refer to electrical characteristics)
VSS	Source ground, connected to 0V
VCAP_1~2	Core voltage, connected to VSS pin to stabilize core voltage (refer to electrical characteristics)
AVCC	Analog power supply, supply power to the analog module, connect to the same voltage as VCC (refer to electrical characteristics) When not using the analog module, please short-circuit with VCC
AVSS/VREFL	Analog power ground/reference voltage, connected to the same voltage as AVSS (refer to electrical characteristics) When not using the analog module, please short-circuit with VSS
VREFH	ADC1, ADC2 analog reference voltage, connect to a voltage not higher than AVCC When not using ADC, please short-circuit with AVCC
PB11/MD	Mode input, fixed to input state. When the reset pin (NRST) is released (from low to high), this pin must be fixed to high. It is recommended to connect resistance (4.7KΩ) to VCC (pull up)
NRST	Reset pin, low effective. Connect resistance to VCC when not in use (pull up)
Pxy, x=A~E,H, y=0~15	General pin. Input voltage should not exceed 5V when used as input function. When used as an analog input, the analog voltage should not exceed VREFH/AVCC Leave it open when not in use, or connect a resistor to VCC (pull up)/VSS (pull down)

Table2 - 6 Pin description

3 Electrical characteristics (ECs)

3.1 Parameter conditions

All voltages are VSS-based unless otherwise specified.

3.1.1 Minimum and maximum

Unless otherwise specified, the minimum and maximum values of all devices are guaranteed by design or performance tests at worst ambient temperature, supply voltage and clock frequency.

3.1.2 Typical value

Unless otherwise specified, typical data are obtained through design or characteristic test analysis under the conditions of T_A = 25 °C and VCC = 3.3 V.

3.1.3 Typical curve

Unless otherwise specified, all typical curves are not tested for design reference only.

3.1.4 Load capacitance

Figure3 -1 (Left) shows the load conditions used to measure the pin parameters.

3.1.5 Pin input voltage

Figure3 -1 (Right) shows the method of measuring the input voltage on the pin of the device.

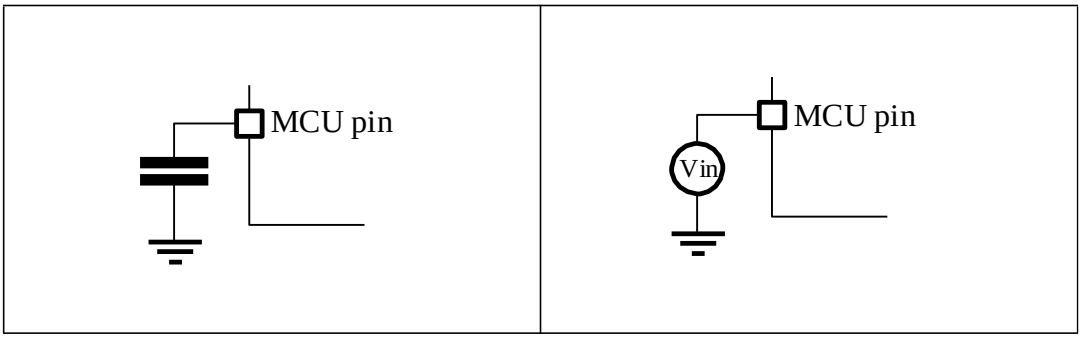


Figure3 -1 Pin load condition (left) and input voltage Measurement (right)

3.1.6 Power supply scheme

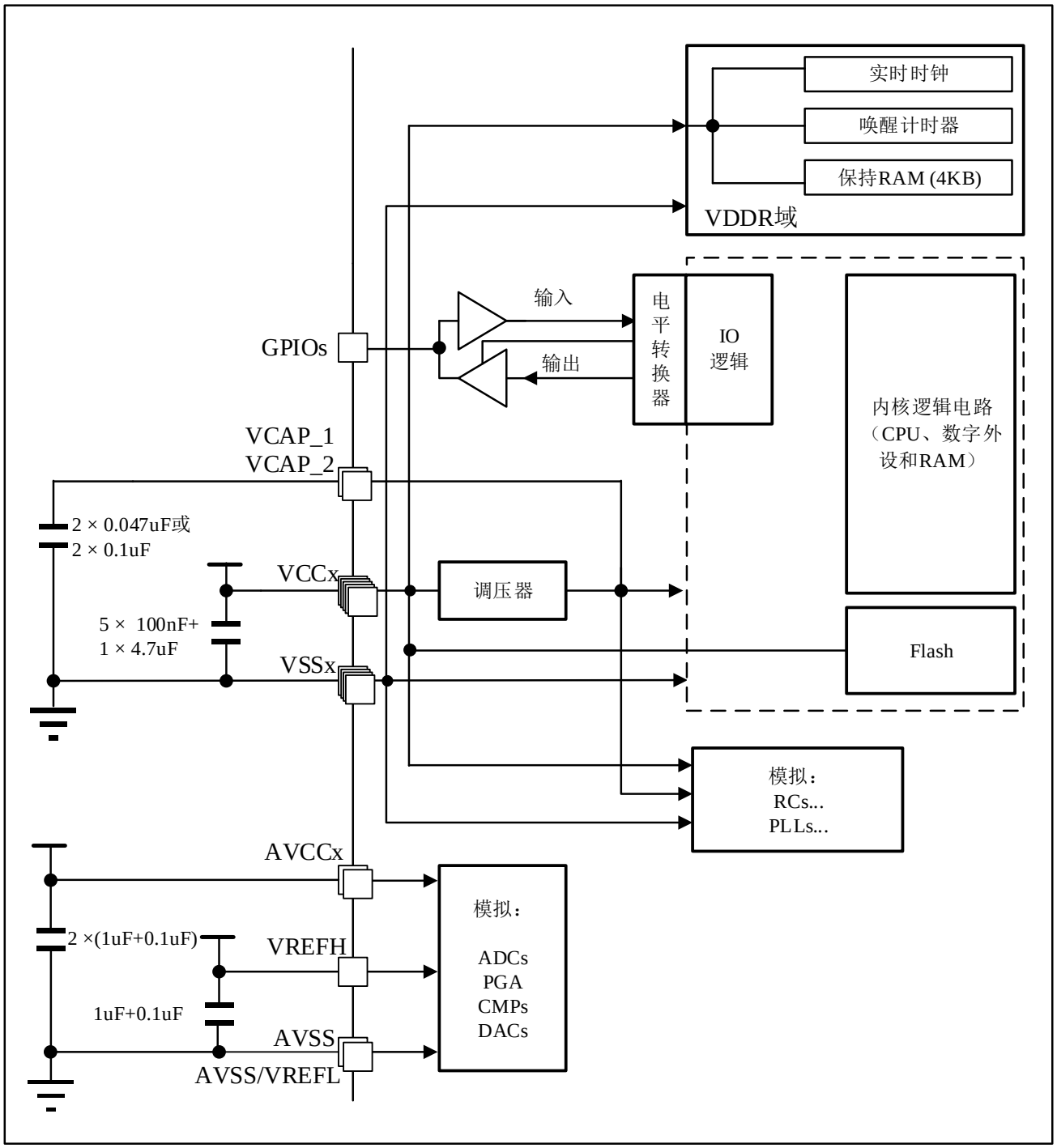


Figure3 -2 Power scheme (HC32F460PETB-LQFP100 , HC32F460PEHB-VFBGA100)

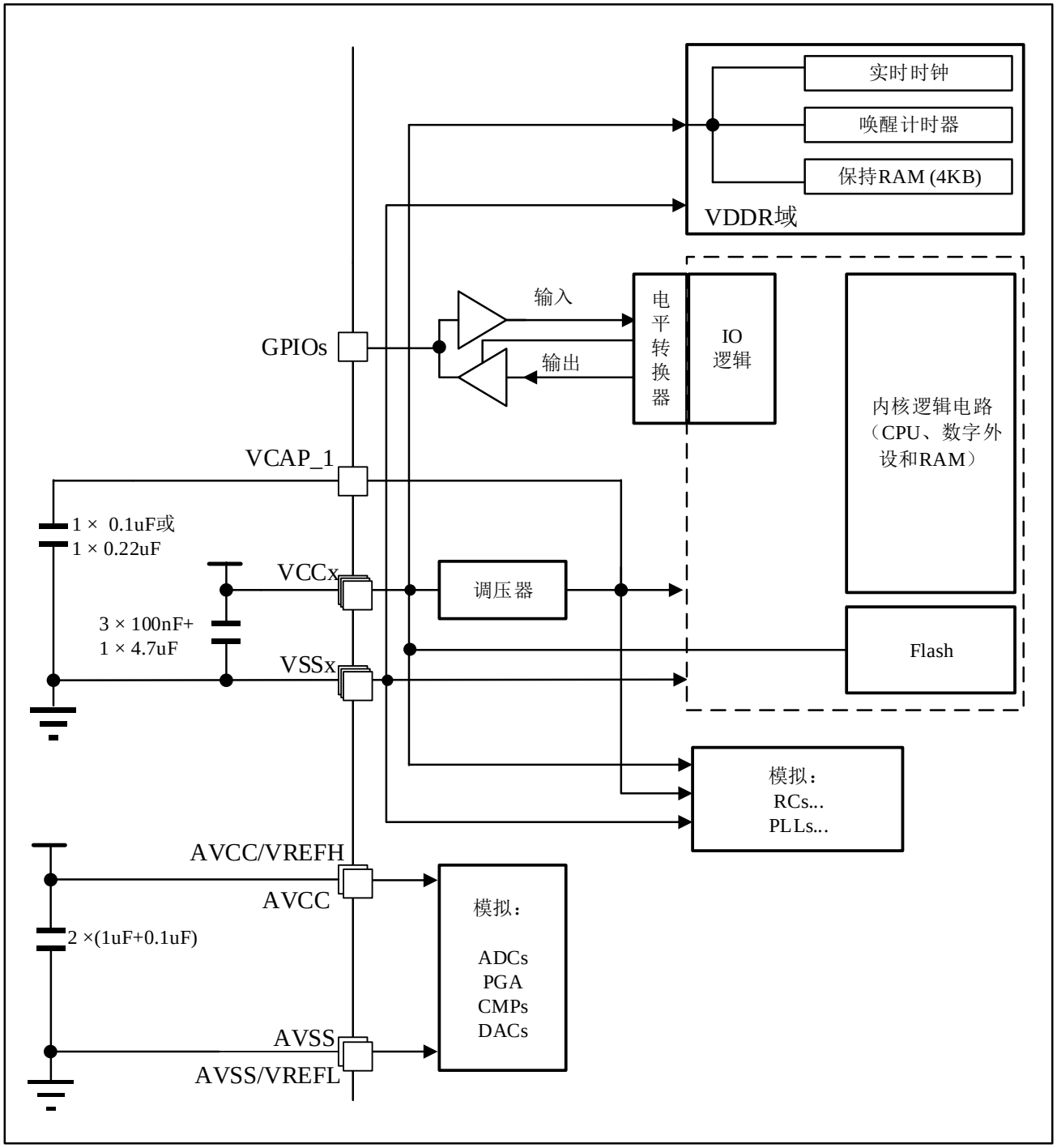


Figure3 -3 Power solution (HC32F460KETA-LQFP64)

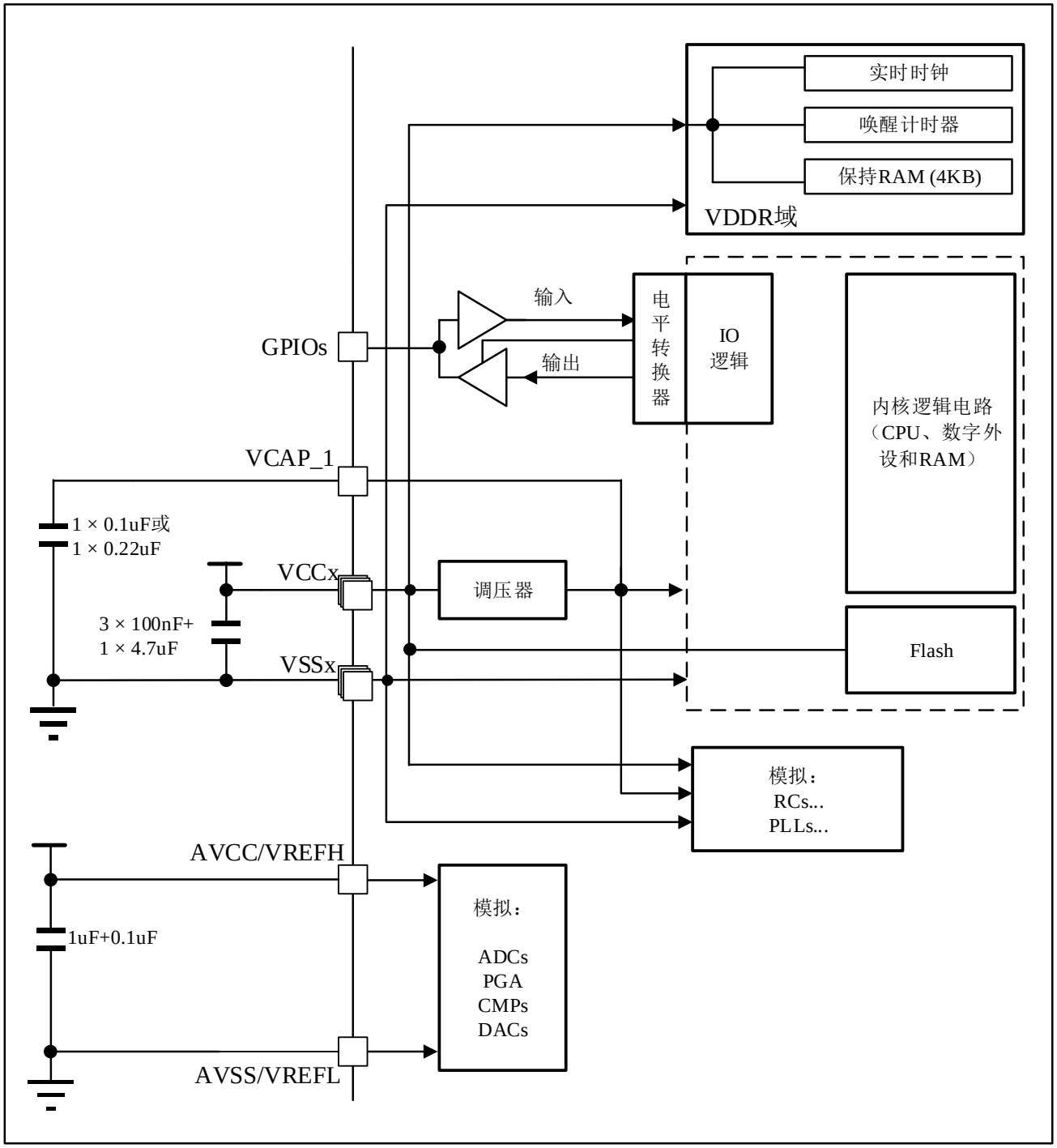


Figure3 - 4 Power solution (HC32F460KEUA-QFN60TR/HC32F460JETA-LQFP48/HC32F460JEUA-QFN48TR)

1. A 4.7μF ceramic capacitor must be connected to one of the VCC pins.
2. AVSS=VSS.
3. Each power supply pair (eg VCC/VSS, AVCC/AVSS...) The filter ceramic capacitor described above must be used for decoupling. These capacitors must be as close as possible or lower than the appropriate pins under the PCB to ensure normal operation of the device. Filtering capacitors are not

recommended to reduce PCB size or cost. This may result in abnormal operation of the device.

4. The capacitors used by the VCAP_1/VCAP_2 pins of the chip are as follows: 1) For chips with both VCAP_1 and VCAP_2 pins, each pin can use 0.047uF or 0.1uF capacitors (total capacity is 0.094uF or 0.2uF). 2) For chips with only VCAP_1 pin, 0.1uF or 0.22uF capacitors can be used. When waking up from power-down mode, VCAP_1/VCAP_2 needs to be charged during the core voltage establishment process. On the one hand, the smaller total capacity of VCAP_1/VCAP_2 can shorten the charging time and bring fast response to the application; on the other hand, the larger total capacity of VCAP_1/VCAP_2 will extend the charging time, but also provide stronger electromagnetic compatibility (EMC). Users can choose a larger or smaller capacitance value according to the requirements of electromagnetic compatibility and system response speed. The total capacity of the chip's VCAP_1/VCAP_2 must match the assignment of the PWC_PWRC3.PDTS bit. When the total capacity of VCAP_1/VCAP_2 is 0.2uF or 0.22uF, you need to ensure that the PWC_PWRC3.PDTS bit is cleared before entering the power-down mode. When the total capacity of VCAP_1/VCAP_2 is 0.094uF or 0.1uF, you need to ensure that the PWC_PWRC3.PDTS bit is set before entering the power-down mode.
5. The stability of the main voltage regulator is achieved by connecting an external capacitor to the VCAP_1 (or VCAP_1/VCAP_2) pin. The capacitance value is C_{EXT} Determined according to the stability requirements of the system. Capacitance value C_{EXT} And ESR requirements are as follows:

Symbol	Parameter	Conditions
C_{EXT}	Capacitance value of external capacitance	0.047μF / 0.1μF / 0.22uF
ESR	Equivalent series resistance ESR of external	<0.3 Ω

Table3 -1 VCAP_1/VCAP_2 working conditions

3.1.7 Current consumption measurement

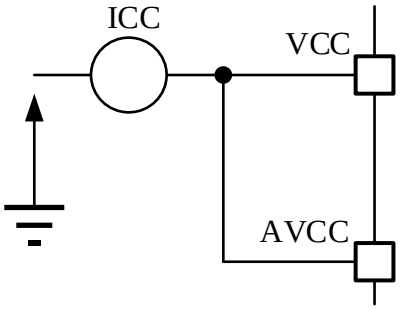


Figure3 -5 Current consumption measurement scheme

3.2 Absolute maximum ratings

If the load on the device exceeds Table3-2 Voltage characteristics , Table3-3 Current characteristics withTable3 -4 Thermal characteristics The absolute maximum ratings listed in may cause permanent damage to the device. These values are just rated stresses and do not mean that the device works properly under these conditions. Long-term operation may affect the reliability .

Symbol	Item	Min	Max	Unit
V_{CC} -V_{SS}	External main power supply voltage (including	-0.3	4.0	V
V_{IN}	Input voltage on the 5V withstand voltage pin (2)	V_{SS} –0.3	VCC+4.0 (maximum 5.8V)	
	Input voltage on PA11/USBFS_DM and PA12/USBFS_DP pins	V_{SS} –0.3	4.0	
$V_{ESD(HBM)}$	Electrostatic discharge voltage(mannequin)	Please refer to3.3.5Electrical		-

Table3-2 Voltage characteristics

1. Within the allowable range, all main power (VCC, AVCC) and ground (VSS, AVSS) pins must always be connected to an external power supply.
2. The maximum value of VIN must always be followed. For information on the maximum allowable injection current value, see Table3-3 .

Symbol	Item	Max	Unit
ΣI_{VCC}	Total current flowing into all VCC X power lines (source current) (1)	240	mA
ΣI_{VSS}	The total current flowing out of all VSS X ground wires (sink current)	-240	
I_{VCC}	Maximum current flowing into each VCC X power line (source current)	100	
I_{VSS}	Maximum current flowing out of each VSS X ground wire (sink	-100	
I_{IO}	Arbitrary I/O and control pin output current	40	
	Output pull current of any I/O and control pin	-40	
ΣI_{IO}	Total output sink current on all I/O and control pins	120	
	Total output current sourced on all I/O and control pins	-120	

Table3-3 Current characteristics

1. Within the allowable range, all main power (VCC, AVCC) and ground (VSS, AVSS) pins must always be connected to an external power supply.

Symbol	Item	Value	Unit
T_{STG}	Storage temperature range	–55 to +125	°C
TJ	Maximum junction temperature	125	°C

Table3 -4 Thermal characteristics

3.3 Operating conditions

3.3.1 General operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
fHCLK	Internal AHB clock frequency	Ultra high speed mode [1] PWRC2.DVS=00 PWRC2.DDAS=1111	0	-	200	MHz
		High speed mode [1] PWRC2.DVS=11 PWRC2.DDAS=1111	0	-	168	
		Ultra low speed mode PWRC2.DVS=10 PWRC2.DDAS=1000	0	-	8	
VCC	Standard operating	-	1.8	-	3.6	V
V_{AVCC} (2)	Analog working voltage	-	1.8	-	3.6	
V_{IN}	Input voltage on the 5V withstand voltage pin (3)	2 V ≤ VCC ≤ 3.6 V	–0.3	-	5.5	
		VCC ≤ 2 V	–0.3	-	5.2	
	PA11/USBFS_DM PA12/USBFS_DP Pin input voltage		–0.3	-	VCC+0.3	
TJ	Junction temperature		-40	-	125	°C

Table3-5 General working conditions

1. Guarantee of mass production test.
2. If there is a VREFH pin, the following conditions must be considered: V_{AVCC} -V_{REFH} <1.2 V.
3. To keep the voltage above V_{CC} +0.3, the internal pull-up/pull-down resistors must be disabled.

3.3.2 Operationg conditions in case of power-on/power-off

TA obeys general operating conditions.

Symbol	Parameter	Min	Max	Unit
t_{VCC}	VCC rise time rate	20	20000	μs/V
	VCC fall time rate	20	20000	

Table3 -6 Working conditions at power-up/power-down

3.3.3 Reset and power control module characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{BOR}	BOR monitoring voltage	Ultra high speed	ICG1.BOR_LEV[1:0]=00	1.88	1.99	2.09	V
			ICG1.BOR_LEV [1:0]=01	1.99	2.09	2.20	V
			ICG1.BOR_LEV [1:0]=10	2.09	2.20	2.30	V
			ICG1.BOR_LEV [1:0]=11	2.30	2.40	2.51	V
		High speed Ultra low speed	ICG1.BOR_LEV[1:0]=00	1.80	1.90	2.00	V
			ICG1.BOR_LEV [1:0]=01	1.90	2.00	2.10	V
			ICG1.BOR_LEV [1:0]=10	2.00	2.10	2.20	V
			ICG1.BOR_LEV [1:0]=11	2.20	2.30	2.40	V
V_{PVD1}	PVD1 monitoring voltage (3)	Ultra high speed	PVD1LVL[2:0]=000	1.99	2.09	2.20	V
			PVD1LVL[2:0]=001	2.09	2.20	2.30	V
			PVD1LVL[2:0]=010	2.30	2.40	2.51	V
			PVD1LVL[2:0]=011	2.54	2.67	2.79	V
			PVD1LVL[2:0]=100	2.65	2.77	2.90	V
			PVD1LVL[2:0]=101	2.75	2.88	3.00	V
			PVD1LVL[2:0]=110	2.85	2.98	3.11	V
			PVD1LVL[2:0]=111	2.96	3.08	3.21	V
		High speed mode Ultra low speed	PVD1LVL[2:0]=000	1.90	2.00	2.10	V
			PVD1LVL[2:0]=001	2.00	2.10	2.20	V
			PVD1LVL[2:0]=010	2.20	2.30	2.40	V
			PVD1LVL[2:0]=011	2.43	2.55	2.67	V
			PVD1LVL[2:0]=100	2.53	2.65	2.77	V
			PVD1LVL[2:0]=101	2.63	2.75	2.87	V
			PVD1LVL[2:0]=110	2.73	2.85	2.97	V
			PVD1LVL[2:0]=111	2.83	2.95	3.07	V
V_{PVD2}	PVD2 monitoring voltage (3)	Ultra high speed	PVD2LVL[2:0]=000	2.09	2.20	2.30	V
			PVD2LVL[2:0]=001	2.30	2.40	2.51	V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
			PVD2LVL[2:0]=010	2.54	2.67	2.79	V
			PVD2LVL[2:0]=011	2.65	2.77	2.90	V
			PVD2LVL[2:0]=100	2.75	2.88	3.00	V
			PVD2LVL[2:0]=101	2.85	2.98	3.11	V
			PVD2LVL[2:0]=110	2.96	3.08	3.21	V
			PVD2LVL[2:0]=111 (2)	1.05	1.15	1.25	V
		High speed mode Ultra low speed	PVD2LVL[2:0]=000	2.00	2.10	2.20	V
			PVD2LVL[2:0]=001	2.20	2.30	2.40	V
			PVD2LVL[2:0]=010	2.43	2.55	2.67	V
			PVD2LVL[2:0]=011	2.53	2.65	2.77	V
			PVD2LVL[2:0]=100	2.63	2.75	2.87	V
			PVD2LVL[2:0]=101	2.73	2.85	2.97	V
			PVD2LVL[2:0]=110 (1)	2.83	2.95	3.07	V
			PVD2LVL[2:0]=111 (2)	1.00	1.10	1.20	V
V_{pvd}	Hysteresis of			-	100	-	mV
V_{POR} (1)	Power-on/power-off reset threshold	Rising edge VPOR		1.60	1.68	1.76	V
		Falling edge VPDR		1.56	1.64	1.72	V
V_{POR}	POR hysteresis			-	40	-	mV
I_{RUSH}	Surge current when the voltage regulator is powered on (POR			-	100	150	mA
T_{NRST}	NRST reset			500	-	-	ns
T_{IPVD1}	PVD1 Reset release			300	380	460	μs
T_{IPVD2}	PVD2 Reset release			300	380	460	μs
T_{INRST}	NRST reset release			25	35	50	μs
T_{RIPT}	Internal reset time			140	160	200	μs
T	BOR reset release			440	520	610	μs

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{RSTPOR}	Power-on reset		-	2500	3000	μs

Table3 -7 Reset and power control module features

1. Guarantee of mass production test.
2. When PVD2LVDL[2:0] = 111, the comparison voltage is The external input comparison voltage of the PVD2EXINP pin.
3. The PVD1 monitoring voltage is the monitoring voltage when the VCC voltage drops; when PVD2LVL[2:0] is set to 111, the PVD2 monitoring voltage is the monitoring voltage when the PVDEXINP voltage drops, and when PVD2LVD[2:0] is set to a value other than 111 The PVD2 monitoring voltage is the monitoring voltage when the VCC voltage drops.
4. The hysteresis of PVD1,2 is the difference between the monitor voltage when VCC rises and the monitor voltage when VCC falls.

PVD1 monitoring voltage when VCC rises=Vpvd1+Vpvdhyst;

PVD2 monitoring voltage when VCC rises=Vpvd2+Vpvdhyst.

3.3.4 Supply Current characteristics

The current consumption is affected by several parameters and factors, including operating voltage, ambient temperature, I/O pin load, device software configuration, operating frequency, I/O pin switch rate, program position in memory and running code.

Figure3 -5 Current consumption measurement scheme The measurement method of current consumption is introduced in. The current consumption measurement values in various operating modes described in this section are obtained through a set of test codes running in FLASH under laboratory conditions.

The specific conditions are as follows:

1) All I/O pins are in input mode, with static values on VCC or VSS (no load).
2) Clock frequency selection Ultra-high speed mode f_{HCLK} =200MHz,
   High-speed mode f_{HCLK} =168MHz/120MHz/24MHz and ultra-low-speed mode f_{HCLK} =8MHz/1MHz.
3) The power consumption modes are divided into: Normal working mode ICC_RUN, sleep mode ICC_SLEEP, stop mode ICC_STP, power down mode ICC_PD and Dhrystone working mode ICC_DHRYSTONE.
4) For peripheral clock ON/OFF, please refer to specific current test items.
5) The PLL is turned on in the ultra-high-speed mode f_{HCLK} =200MHz and the high-speed mode f_{HCLK} =168MHz/120MHz.

Pattern	Parameter	Symbol	Conditions	Ta (°C)	Product Specifications			Unit
					Min	Typ (1)	Max (2)	
Ultrahigh speed Pattern	f_{HCLK} = 200MHz	ICC_RUN	While (1), full-module clock OFF	-40	-	16	-	mA
			While (1), full module clock ON	-40	-	29	-	mA
		ICC_DHRYSTONE	CACHE OFF	-40	-	17	-	mA
			CACHE ON	-40	-	19	-	mA
		ICC_SLEEP	Full module clock OFF	-40	-	11	-	mA
			Full module clock ON	-40	-	24	-	mA
		ICC_RUN	While (1), full-module clock OFF	25	-	16	-	mA
			While (1), full module clock ON	25	-	29	-	mA
		ICC_DHRYSTONE	CACHE OFF	25	-	17	-	mA
			CACHE ON	25	-	19	-	mA
		ICC_SLEEP	Full module clock OFF	25	-	11	-	mA
			Full module clock ON	25	-	24	-	mA
		ICC_RUN	While (1), full-module clock OFF	85	-	-	22	mA
			While (1), full module clock ON	85	-	-	35	mA
		ICC_DHRYSTONE	CACHE OFF	85	-	-	22	mA
			CACHE ON	85	-	-	25	mA
		ICC_SLEEP	Full module clock OFF	85	-	-	17	mA
			Full module clock ON	85	-	-	30	mA
		ICC_RUN	While (1), full-module clock OFF	105	-	-	25	mA
			While (1), full module clock ON	105	-	-	39	mA
		ICC_DHRYSTONE	CACHE OFF	105	-	-	24	mA
			CACHE ON	105	-	-	29	mA
		ICC_SLEEP	Full module clock OFF	105	-	-	21	mA
			Full module clock ON	105	-	-	34	mA

Table3 - 8 Ultra-high-speed mode current consumption

1. Typ voltage condition V_{CC} =3.3V
2. Max voltage condition V_{CC} =1.8~3.6V

Pattern	Parameter	Symbol	Conditions	Ta (°C)	Product Specifications			Unit
					Min	Typ (1)	Max (2)	
high speed Pattern	f_{HCLK} = 168MHz	ICC_RUN	While (1), full-module clock OFF	-40	-	13	-	mA
			While (1), full module clock ON	-40	-	23	-	mA
		ICC_DHRYSTONE	CACHE OFF	-40	-	14	-	mA
			CACHE ON	-40	-	15	-	mA
		ICC_SLEEP	Full module clock OFF	-40	-	9	-	mA
			Full module clock ON	-40	-	19	-	mA
		ICC_RUN	While (1), full-module clock OFF	25	-	13	-	mA
			While (1), full module clock ON	25	-	23	-	mA
		ICC_DHRYSTONE	CACHE OFF	25	-	14	-	mA
			CACHE ON	25	-	15	-	mA
		ICC_SLEEP	Full module clock OFF	25	-	9	-	mA
			Full module clock ON	25	-	19	-	mA
		ICC_RUN	While (1), full-module clock OFF	85	-	-	18	mA
			While (1), full module clock ON	85	-	-	28	mA
		ICC_DHRYSTONE	CACHE OFF	85	-	-	18	mA
			CACHE ON	85	-	-	20	mA
		ICC_SLEEP	Full module clock OFF	85	-	-	14	mA
			Full module clock ON	85	-	-	24	mA
		ICC_RUN	While (1), full-module clock OFF	105	-	-	20	mA
			While (1), full module clock ON	105	-	-	31	mA
		ICC_DHRYSTONE	CACHE OFF	105	-	-	19	mA

			CACHE ON	105	-	-	23	mA
		ICC_SLEEP	Full module clock OFF	105	-	-	17	mA
			Full module clock ON	105	-	-	27	mA

Table3-9 High-speed mode current consumption 1

1. Typ voltage condition V_{CC} =3.3V
2. Max voltage condition V_{CC} =1.8~3.6V

Pattern	Parameter	Symbol	Conditions	Ta (°C)	Product Specifications			Unit
					Min	Typ (1)	Max (2)	
high speed Pattern	f_{HCLK} = 120MHz	ICC_RUN	While (1), full-module clock OFF	-40	-	9.5	-	mA
			While (1), full module clock ON	-40	-	16.5	-	mA
		ICC_DHRYSTONE	CACHE OFF	-40	-	10	-	mA
			CACHE ON	-40	-	11.5	-	mA
		ICC_SLEEP	Full module clock OFF	-40	-	7	-	mA
			Full module clock ON	-40	-	14.5	-	mA
		ICC_RUN	While (1), full-module clock OFF	25	-	9.5	-	mA
			While (1), full module clock ON	25	-	16.5	-	mA
		ICC_DHRYSTONE	CACHE OFF	25	-	10	-	mA
			CACHE ON	25	-	11.5	-	mA
		ICC_SLEEP	Full module clock OFF	25	-	7	-	mA
			Full module clock ON	25	-	14.5	-	mA
		ICC_RUN	While (1), full-module clock OFF	85	-	-	14	mA
			While (1), full module clock ON	85	-	-	22	mA
		ICC_DHRYSTON	CACHE OFF	85	-	-	14	mA

		E	CACHE ON	85	-	-	17	mA
		ICC_SLEEP	Full module clock OFF	85	-	-	12	mA
			Full module clock ON	85	-	-	20	mA
		ICC_RUN	While (1), full-module clock OFF	105	-	-	16	mA
			While (1), full module clock ON	105	-	-	25	mA
		ICC_DHRYSTON E	CACHE OFF	105	-	-	15	mA
			CACHE ON	105	-	-	19	mA
		ICC_SLEEP	Full module clock OFF	105	-	-	15	mA
			Full module clock ON	105	-	-	22	mA

Table3 - 10 High-speed mode current consumption 2

1. Typ voltage condition V_{CC} =3.3V
2. Max voltage condition V_{CC} =1.8~3.6V

Pattern	Parameter	Symbol	Conditions	Ta (°C)	Product Specifications			Unit
					Min	Typ (1)	Max (2)	
high speed Pattern	f_{HCLK} = 24MHz	ICC_RUN	While (1), full-module clock OFF	-40	-	3	-	mA
			While (1), full module clock ON	-40	-	6	-	mA
		ICC_DHRYSTONE	CACHE OFF	-40	-	3.5	-	mA
		ICC_SLEEP	Full module clock OFF	-40	-	2	-	mA
			Full module clock ON	-40	-	5.5	-	mA
		ICC_RUN	While (1), full-module clock OFF	25	-	3	-	mA
			While (1), full module clock ON	25	-	6	-	mA
		ICC_DHRYSTONE	CACHE OFF	25	-	3.5	-	mA
		ICC_SLEEP	Full module clock OFF	25	-	2	-	mA
			Full module clock ON	25	-	5.5	-	mA
		ICC_RUN	While (1), full-module clock OFF	85	-	-	8	mA
			While (1), full module clock ON	85	-	-	12	mA
		ICC_DHRYSTONE	CACHE OFF	85	-	-	7	mA
		ICC_SLEEP	Full module clock OFF	85	-	-	8	mA
			Full module clock ON	85	-	-	11	mA
		ICC_RUN	While (1), full-module clock OFF	105	-	-	10	mA
			While (1), full module clock ON	105	-	-	14	mA
		ICC_DHRYSTONE	CACHE OFF	105	-	-	8	mA
		ICC_SLEEP	Full module clock OFF	105	-	-	10	mA
			Full module clock ON	105	-	-	14	mA

Table3 - 11 High-speed mode current consumption 3

1. Typ voltage condition V_{CC} =3.3V
2. Max voltage condition V_{CC} =1.8~3.6V

Pattern	Parameter	Symbol	Conditions	Ta (°C)	Product Specifications			Unit
					Min	Typ (1)	Max (2)	
Ultra low speed Pattern	f_{HCLK} = 8MHz	ICC_RUN	While (1), full-module clock OFF	-40	-	1	-	mA
			While (1), full module clock ON	-40	-	3.5	-	mA
		ICC_DHRYSTONE	CACHE OFF	-40	-	1.5	-	mA
		ICC_SLEEP	Full module clock OFF	-40	-	1.2	-	mA
			Full module clock ON	-40	-	3.2	-	mA
		ICC_RUN	While (1), full-module clock OFF	25	-	1	-	mA
			While (1), full module clock ON	25	-	3.5	-	mA
		ICC_DHRYSTONE	CACHE OFF	25	-	1.5	-	mA
		ICC_SLEEP	Full module clock OFF	25	-	1.2	-	mA
			Full module clock ON	25	-	3.2	-	mA
		ICC_RUN	While (1), full-module clock OFF	85	-	-	4	mA
			While (1), full module clock ON	85	-	-	6	mA
		ICC_DHRYSTONE	CACHE OFF	85	-	-	4	mA
		ICC_SLEEP	Full module clock OFF	85	-	-	3.5	mA
			Full module clock ON	85	-	-	6	mA
		ICC_RUN	While (1), full-module clock OFF	105	-	-	6	mA
			While (1), full module clock ON	105	-	-	7	mA
		ICC_DHRYSTONE	CACHE OFF	105	-	-	4.5	mA
		ICC_SLEEP	Full module clock OFF	105	-	-	4	mA
			Full module clock ON	105	-	-	6.5	mA

Table3 - 12 Ultra-low speed mode current consumption 1

1. Typ voltage condition V_{CC} =3.3V
2. Max voltage condition V_{CC} =1.8~3.6V

Pattern	Parameter	Symbol	Conditions	Ta (°C)	Product Specifications			Unit
					Min	Typ (1)	Max (2)	
Ultra low speed Pattern	f_{HCLK} = 1MHz	ICC_RUN	While (1), full-module clock OFF	-40	-	0.7	-	mA
			While (1), full module clock ON	-40	-	2.5	-	mA
		ICC_DHRYSTONE	CACHE OFF	-40	-	0.9	-	mA
		ICC_SLEEP	Full module clock OFF	-40	-	0.9	-	mA
			Full module clock ON	-40	-	2.4	-	mA
		ICC_RUN	While (1), full-module clock OFF	25	-	0.7	-	mA
			While (1), full module clock ON	25	-	2.5	-	mA
		ICC_DHRYSTONE	CACHE OFF	25	-	0.9	-	mA
		ICC_SLEEP	Full module clock OFF	25	-	0.9	-	mA
			Full module clock ON	25	-	2.4	-	mA
		ICC_RUN	While (1), full-module clock OFF	85	-	-	4	mA
			While (1), full module clock ON	85	-	-	5	mA
		ICC_DHRYSTONE	CACHE OFF	85	-	-	3.5	mA
		ICC_SLEEP	Full module clock OFF	85	-	-	3.5	mA
			Full module clock ON	85	-	-	5	mA
		ICC_RUN	While (1), full-module clock OFF	105	-	-	5	mA
			While (1), full module clock ON	105	-	-	5.5	mA
		ICC_DHRYSTONE	CACHE OFF	105	-	-	4	mA
		ICC_SLEEP	Full module clock OFF	105	-	-	5	mA
			Full module clock ON	105	-	-	5.5	mA

Table3 - 13 Ultra low speed mode current consumption 2

1. Typ voltage condition V_{CC} =3.3V
2. Max voltage condition V_{CC} =1.8~3.6V

Pattern	Parameter	Symbol	Conditions (VCC=3.3V)	Ta (°C)	Product Specifications			Unit
					Min	Typ (1)	Max (2)	
Stop mode	-	ICC_STP	PWC_PWRC1.STPDAS=00	-40	-	160	-	uA
			PWC_PWRC1.STPDAS=11	-40	-	30	-	uA
			PWC_PWRC1.STPDAS=00	25	-	220	-	uA
			PWC_PWRC1.STPDAS=11	25	-	80	-	uA
			PWC_PWRC1.STPDAS=00	85	-	-	3600	uA
			PWC_PWRC1.STPDAS=11	85	-	-	3400	uA
			PWC_PWRC1.STPDAS=00	105	-	-	4800	uA
			PWC_PWRC1.STPDAS=11 (3)	105	-	-	4600	uA
Power down mode	-	ICC_PD	Power down mode 1	-40	-	10	-	uA
			Power down mode 2	-40	-	4	-	uA
			Power down mode 3	-40	-	1.8	-	uA
			Power down mode 4	-40	-	1.8	-	uA
			Power down mode 2+XTAL32+RTC	-40	-	6	-	uA
			Power down mode 2+LRC+RTC	-40	-	9	-	uA
			Power down mode 1	25	-	10	-	uA
			Power down mode 2	25	-	4	-	uA
			Power down mode 3	25	-	1.8	-	uA
			Power down mode 4	25	-	1.8	-	uA
			Power down mode 2+XTAL32+RTC	25	-	6	-	uA
			Power down mode 2+LRC+RTC	25	-	9	-	uA
			Power down mode 1	85	-	-	21	uA
			Power down mode 2	85	-	-	19	uA
			Power down mode 3	85	-	-	19	uA
			Power down mode 4	85	-	-	19	uA

Pattern	Parameter	Symbol	Conditions (VCC=3.3V)	Ta (°C)	Product Specifications			Unit
					Min	Typ (1)	Max (2)	
			Power down mode 2+XTAL32+RTC	85	-	-	21	uA
			Power down mode 2+LRC+RTC	85	-	-	21	uA
			Power down mode 1	105	-	-	35	uA
			Power down mode 2	105	-	-	33	uA
			Power down mode 3	105	-	-	30	uA
			Power down mode 4 [3]	105	-	-	30	uA
			Power down mode 2+XTAL32+RTC	105	-	-	35	uA
			Power down mode 2+LRC+RTC	105	-	-	35	uA

Table3-14 Low power consumption mode current consumption

1. Typ voltage condition V_{CC} =3.3V
2. Max voltage condition V_{CC} =1.8~3.6V
3. Guarantee of mass production test.

Item	Parameter	Symbol	Conditions (VCC=AVCC=3.3V)	Ta (°C)	Product Specifications			Unit
					Min	Typ	Max	
Modules Current	-	ICC_MODULE	XTAL oscillation mode large drive 24MHz	25	-	1.8	-	mA
			Drive 16 MHz in Oscillation Mode	25	-	1	-	mA
			Oscillation mode small drive 10MHz	25	-	0.8	-	mA
			Oscillation mode ultra-small drive 8MHz	25	-	0.6	-	mA
			XTAL 32K	25	-	0.5	-	mA
			HRC	25	-	0.35	-	mA
			PLL (@480MHz)	25	-	2.3	-	mA
			PLL (@240MHz)	25	-	1.4	-	mA

Item	Parameter	Symbol	Conditions (VCC=AVCC=3.3V)	Ta (°C)	Product Specifications			Unit
					Min	Typ	Max	
			ADC	25	-	1.2	-	mA
			DAC	25	-	70	-	uA
			CMP	25	-	0.11	-	mA
			PGA	25	-	1	-	mA
			USBFS (1)	25	-	6	-	mA

Table3-15 Analog module current consumption

1. Contains the current when the control part communicates with the USBPHY.

3.3.5 Electrical sensitivity

The chip is tested differently (ESD, LU) using specific measurements to determine its electrical sensitivity performance.

3.3.5.1 Electrostatic discharge (ESD)

Electrostatic discharge is applied to the pins of each sample according to each pin combination. This test complies with JESD22-A114/C101 standard.

Symbol	Parameter	Conditions	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage	TA = + 25 ° C, compliant with JESD22-A114	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charging equipment model)	TA = + 25 ° C, compliant with JESD22-C101	1000	

Table3 - 16 ESD characteristics

3.3.5.2 Static Latch-up

To assess static Latch-up performance, two complementary static Latch-up tests are required on the chip:

- Over-voltage applied to each power supply and analog input pin
- Apply current injection to other input, output and configurable I/O pins

These tests met the EIA/JESD 78A IC Latch-up standard.

Symbol	Parameter	Conditions	Max	Unit
LU	Static Latch-up	T_A = +105 °C, in line with JESD78A	200	mA

Table3 - 17 Static Latch-up feature

3.3.6 Low power mode wake-up timing

The wake-up time measurement method is from the wake-up event triggering to the CPU execution of the first instruction:

- For stop or sleep mode: The wake-up event is WFE.
- WKUP pins are used to wake up from standby, stop, and sleep modes. All timings are tested at ambient temperature and VCC=3.3V.

Symbol	Parameter	Conditions	Typ	Max	Unit
T_{STOP1}	Wakeup from stop mode	PWC_PWRC1.VHRCSD=1 and PWC_PWRC1.VPLLSD=1, the system clock is MRC, and the program is executed on RAM	2	5	us
T_{STOP2}	Wakeup from stop mode	The system clock is MRC, and the program is executed on Flash	8	15	
T_{PD1} (1)	Wake up from power down mode 1	The total capacity of VCAP_1/VCAP_2 is 0.094uF or 0.1uF	15	25	
		The total capacity of VCAP_1/VCAP_2 is 0.2uF or 0.22uF	20	30	
T_{PD2} (1)	Wake up from power down mode 2	The total capacity of VCAP_1/VCAP_2 is 0.094uF or 0.1uF	40	50	
		The total capacity of VCAP_1/VCAP_2 is 0.2uF or 0.22uF	45	55	
T_{PD3} (1)	Wake up from power down mode 3	The total capacity of VCAP_1/VCAP_2 is 0.094uF or 0.1uF	2500	3000	
		The total capacity of VCAP_1/VCAP_2 is 0.2uF or 0.22uF	2500	3000	
T_{PD4} (1)	Wake up from power down mode 4	The total capacity of VCAP_1/VCAP_2 is 0.094uF or 0.1uF	65	75	
		The total capacity of VCAP_1/VCAP_2 is 0.2uF or 0.22uF	70	80	

Table3 - 18 Low power mode wake-up time

1. The total capacity of the chip's VCAP_1/VCAP_2 must match the assignment of the

PWC_PWRC3.PDTS bit. When the total capacity of VCAP_1/VCAP_2 is 0.2uF or 0.22uF, you need to ensure that the PWC_PWRC3.PDTS bit is cleared before entering the power-down mode. When the total capacity of VCAP_1/VCAP_2 is 0.094uF or 0.1uF, you need to ensure that the PWC_PWRC3.PDTS bit is set before entering the power-down mode.

3.3.7 I/O port characteristics

General input/output characteristics

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{IL} (1)	Input low level		1.8≤V_{CC}≤3.6	-	-	0.2V_{CC}	V
V_{IH} (1)	Input high level		1.8≤V_{CC}≤3.6	0.8V_{CC}	-	-	V
V_{HYS}	Input hysteresis		1.8≤V_{CC}≤3.6	-	0.2	-	V
I_{LKG} (1)	I/O input leakage current		V_{SS}≤V_{IN}≤V_{CC}	-	-	1	uA
			V_{IN} = 5.5V (2)	-	-	5	uA
R_{PU} (1)	Weak pull-up equivalent resistance	USBFS_DP, USBFS_DM	-	-	1.5	-	KΩ
		In addition to the other input pins of USBFS_DP and USBFS_DM	V_{IN} = V_{SS}	-	30	-	KΩ
C_{IO}	I/O pin capacitance	PA11/USBFS_DM PA12/USBFS_DP	-	-	10	-	pF
		In addition to other input pins of PA11/USBFS_DM and PA12/USBFS_DP	-	-	5	-	pF

Table3-19 I/O static characteristics

1. Guarantee of mass production test.
2. To keep the voltage higher than V_{CC} +0.3 V, the internal pull-up/pull-down resistors must be disabled.

The output voltage

Drive settings	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Low drive	V_{OL} (1)(2)	Low level output	I_{IO} =± 1.5mA, 1.8≤V_{CC} <2.7	-	-	0.4	V
	V_{OH} (1)(3)	High level output		V_{CC} - 0.4	-	-	
	V_{OL} (1)(2)	Low level output	I_{IO} =± 3mA, 2.7≤V_{CC} ≤3.6	-	-	0.4	
	V_{OH} (1)(3)	High level output		V_{CC}- 0.4	-	-	
	V_{OL} (1)(2)	Low level output	I_{IO} =± 6mA, 2.7≤V_{CC} ≤3.6	-	-	1.3	
	V_{OH} (1)(3)	High level output		V_{CC} - 1.3	-	-	
Medium drive	V_{OL} (1)(2)	Low level output	I_{IO} =± 3mA, 1.8≤V_{CC} <2.7	-	-	0.4	
	V_{OH} (1)(3)	High level output		V_{CC} - 0.4	-	-	
	V_{OL} (1)(2)	Low level output	I_{IO} =± 5mA, 2.7≤V_{CC} ≤3.6	-	-	0.4	
	V_{OH} (1)(3)	High level output		V_{CC} - 0.4	-	-	
	V_{OL} (1)(2)	Low level output	I_{IO} =± 12mA, 2.7≤V_{CC} ≤3.6	-	-	1.3	
	V_{OH} (1)(3)	High level output		V_{CC} - 1.3	-	-	
High drive	V_{OL} (1)(2)	Low level output	I_{IO} =± 6mA, 1.8≤V_{CC} <2.7	-	-	0.4	
	V_{OH} (1)(3)	High level output		V_{CC} - 0.4	-	-	

	V_{OL} (1)(2)	Low level output	I_{IO} =± 8mA, 2.7≤V_{CC} ≤3.6	-	-	0.4	
	V_{OH} (1)(3)	High level output		V_{CC} - 0.4	-	-	
	V_{OL} (1)(2)	Low level output	I_{IO} =± 20mA, 2.7 ≤$V_{CC\leq 3.6}$	-	-	1.3	
	V_{OH} (1)(3)	High level output		V_{CC} - 1.3	-	-	

Table3 - 20 Output voltage characteristics

1. Guarantee of mass production test.
2. The I_{IO} sink current of the device must always be considered Table3-3 Absolute maximum ratings specified in. The sum of IIO (I/O ports and control pins) must not exceed I_{VSS}
3. The $I_{IO\ source}$ current of the device must always follow Table3-3 The absolute maximum ratings listed, the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VCC} .

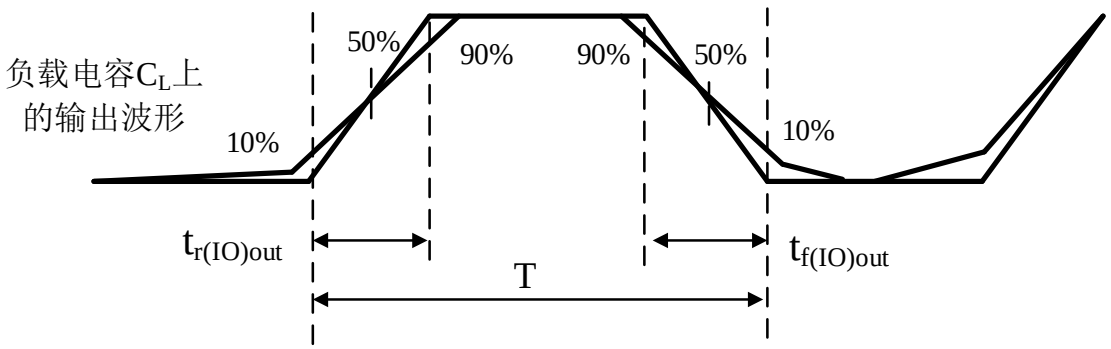
Input/output AC characteristics

Drive settings	Symbol	Parameter	Condition (3)	Min	Typ	Max	Unit
Low drive	f_{max} (IO)out	Maximum frequency (1)	C_L =30 pF, V_{CC} ≥ 2.7V	-	-	20	MHz
			C_L =30 pF, V_{CC} ≥1.8V	-	-	10	
			C_L =10pF, V_{CC} ≥2.7V	-	-	40	
			C_L =10pF, V_{CC} ≥1.8V	-	-	20	
	t_f (IO)out t_r (IO)out	Output high to low level drop time and output low to high level rise time	C_L =30 pF, V_{CC} ≥2.7V	-	-	15	ns
			C_L =30 pF, V_{CC} ≥1.8V	-	-	25	
			C_L =10pF, V_{CC} ≥2.7V	-	-	7.5	
			C_L =10pF, V_{CC} ≥1.8V	-	-	15	
Medium drive	f_{max} (IO)out	Maximum frequency (1)	C_L =30 pF, V_{CC} ≥ 2.7V	-	-	45	MHz
			C_L =30 pF, V_{CC} ≥1.8V	-	-	22.5	
			C_L =10pF, V_{CC} ≥2.7V	-	-	90	
			C_L =10pF, V_{CC} ≥1.8V	-	-	45	
	t_f (IO)out t_r (IO)out	Output high to low level drop time and output low to high level rise time	C_L =30 pF, V_{CC} ≥2.7V	-	-	7.5	ns
			C_L =30 pF, V_{CC} ≥1.8V	-	-	12	
			C_L =10pF, V_{CC} ≥2.7V	-	-	4	
			C_L =10pF, V_{CC} ≥1.8V	-	-	7.5	
High drive	f_{max} (IO)out	Maximum frequency (1)	C_L =30 pF, V_{CC} ≥2.7V	-	-	100	MHz
			C_L =30 pF, V_{CC} ≥1.8V	-	-	50	
			C_L =10pF, V_{CC} ≥2.7V	-	-	180	
			C_L =10pF, V_{CC} ≥1.8V	-	-	100	
	t_f (IO)out t_r (IO)out	Output high to low level drop time and output low to high level rise time	C_L =30 pF, V_{CC} ≥2.7V	-	-	4	ns
			C_L =30 pF, V_{CC} ≥1.8V	-	-	6	
			C_L =10pF, V_{CC} ≥2.7V	-	-	2.5	
			C_L =10pF, V_{CC} ≥1.8V	-	-	4	

Table3 - 21 I/O AC characteristics

1. The maximum frequency is atFigure3 -6 Defined in.
2. The load capacitance C_L must take the capacitance of the PCB and MCU pins into account (the

capacitance of the pins and the circuit board can be roughly estimated as 10 pF).



最大频率条件： $(t_r + t_f) \leqslant (2/3)T$ 并且Duty cycle= 50%±5%（负载电容C_L在“输入/输出交流特性”表格的“条件”一栏中标明）

Figure3 -6 I/O AC characteristic definition

3.3.8 USART Interface Characteristics

Symbol	Parameter		Min	Max	Unit
t_{cyc}	Number of input clock cycles	UART	4	-	t_{PCLK1}
		CSI	6	-	
t_{CKw}	Input clock width		0.4	0.6	t_{Scyc}
t_{CKr}	Input clock rise time		-	5	ns
t_{CKf}	Input clock fall time		-	5	ns
t_{TD}	Send delay time	CSI	-	28	ns
t_{RDS}	Receiving data establishment time	CSI	15	-	ns
t_{RDH}	Receive data hold time	CSI	5	-	ns

Table3 -21 USART AC timing

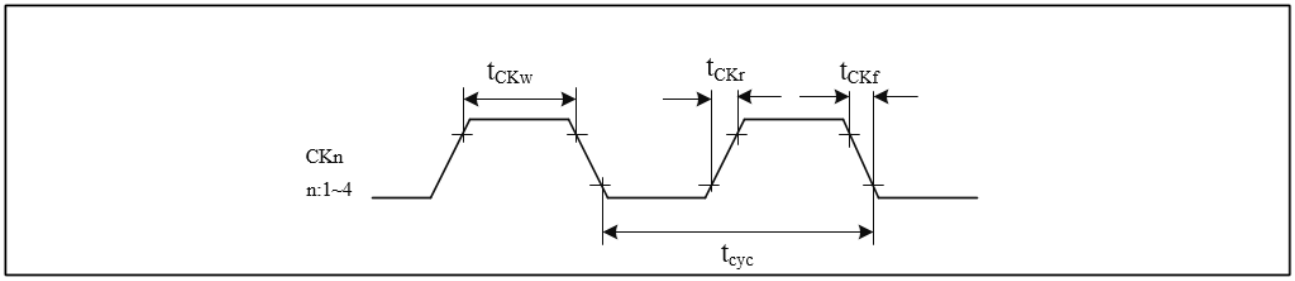


Figure3 -7 USART clock timing

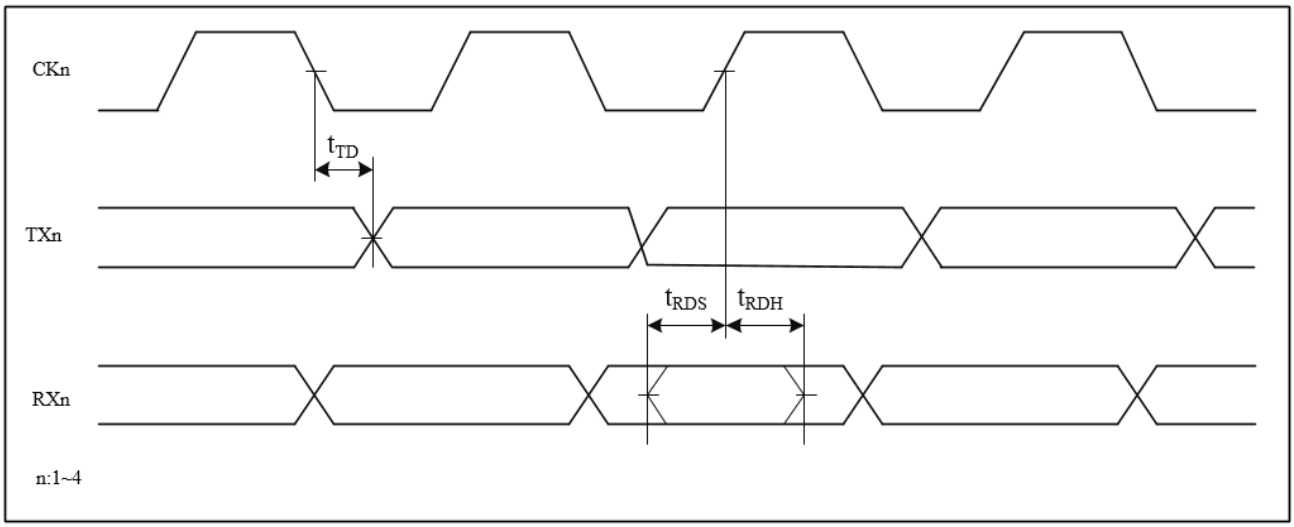


Figure3 -8 USART (CSI) input and output timing

3.3.9 I2S interface characteristics

Symbol	Performance	Conditions	Min	Max	Unit
f_{MCK}	I2S main clock output	-	256 *8K	256*Fs	MHz
f_{CK}	I2S clock frequency	Master data: 32 bits	20	64*Fs	MHz
		Slave data: 32 bits	-	64*Fs	
D_{CK}	I2S clock frequency duty cycle	Slave receiver	30	70	%
t_v (WS)	WS valid time	Master mode	0	-	ns
t_h (WS)	WS hold time	Master mode	0	-	
t_{su} (WS)	WS setup time	Slave mode	1	-	
t_h (WS)	WS hold time	Slave mode	0	-	
t_{su} (SD_MR)	Data input setup time	Master receiver	7.5	-	
t_{su} (SD_SR)		Slave receiver	2	-	
t_h (SD_MR)	Data input hold time	Master receiver	0	-	
t_h (SD_SR)		Slave receiver	0	-	
t_v (SD_ST) t_h (SD_ST)	Data output valid time	Slave transmitter(after enable edge)	-	27	
t_v (SD_MT)		Master transmitter(after enable edge)	-	20	
t_h (SD_MT)	Data output hold time	Master transmitter(after enable edge)	2.5	-	

Table3 - 22 I2S electrical characteristics

1. Fs: I2S sampling frequency

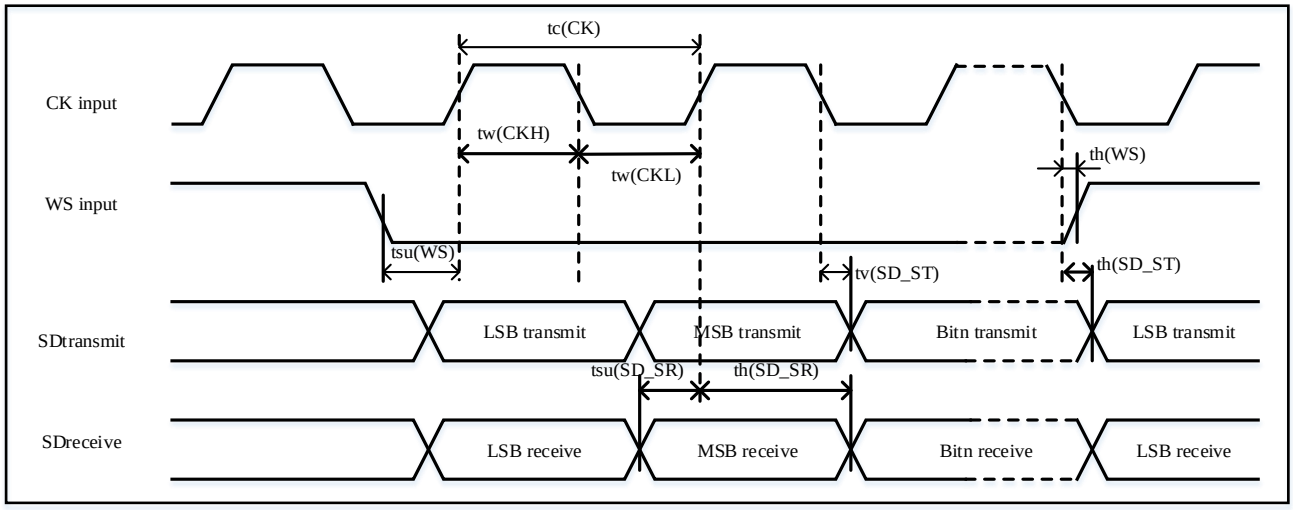


Figure3 -9 I2S slave mode timing (Philips protocol)

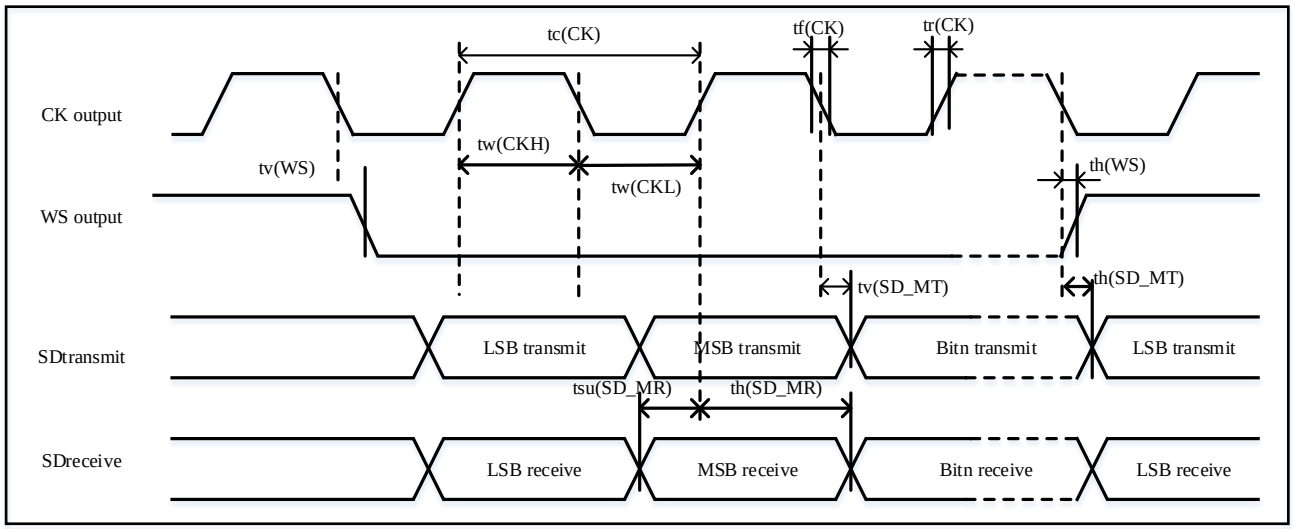


Figure3 -10 I2S master mode timing (Philips protocol)

3.3.10 I2C interface characteristics

Symbol	Parameter	Standard mode (SM)		Fast mode (FM)		Unit
		Min	Max	Min	Max	
f_{SCL}	SCL frequency	0	100	0	400	KHz
$t_{HD;STA}$	Start condition/restart condition Hold	4.0	-	0.6	-	us
t_{LOW}	SCL Low Level	4.7	-	1.3	-	us
t_{HIGH}	SCL High Level	4	-	0.6	-	us
$t_{SU;STA}$	Restarting Condition Setup	4.7	-	0.6	-	us
$t_{HD;DAT}$	Data Hold	0	-	0	-	us
$t_{SU;DAT}$	Data Setup	50+ $t_{I2C\ reference\ clock\ period}$	-	50+ $t_{I2C\ reference\ clock\ period}$	-	ns
t_R	Ascending time of SCL/SDA	-	1000	6.5	300	ns
t_F	Falling time of SCL/SDA	-	300	6.5	300	ns
$t_{SU;STO}$	Stop Condition Setup	4	-	0.6	-	us
tBUF	BUS Idle Time Between Stop Condition and Start Condition	4.7	-	1.3	-	us
C_b	Load capacitance	-	400	-	400	pF

Table3 - 23 I2C electrical characteristics

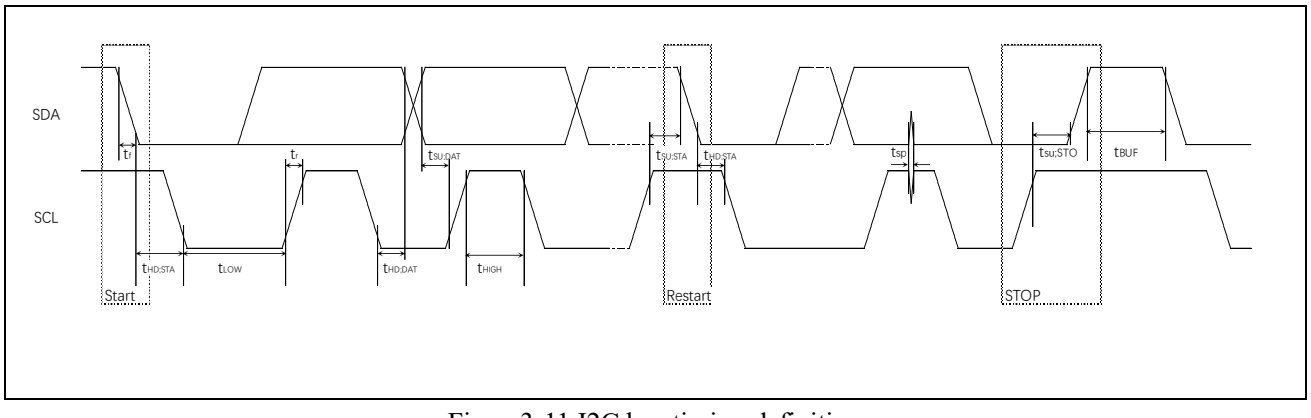


Figure3-11 I2C bus timing definition

3.3.11 SPI Interface Characteristics

Item			Symbol	Min	Max	Unit	Test conditions
	SCK clock cycle	Master	tspcyc	2 (pclk ≤60MHz) 4 (pclk ≤60MHz)	4096	tpcyc	Figure3 -12 C=30pF
		Slave		6	4096		
	SCK clock rise and fall time	Master	tsckr	-	5	ns	
		Slave	tsckf	-	1	us	
	Data input setup time	Master	tsu	4	-	ns	Figure3 -13 C=30pF
		Slave		5	-		
	Data input hold time	Master	th	tpcyc	-	ns	
		Slave		20	-		
	Data output delay	Master	tod	-	8	ns	
		Slave		-	20		
	Data output hold time	Master	toh	0	-	ns	
		Slave		0	-		
	MOSI/MISO rise and fall time	Master	tdr	-	5	ns	
		Slave	tdf	-	1	us	
	SS rise and fall time	Master	tssr	-	5	ns	
		Slave	tssf	-	1	us	

Table3 - 24 SPI electrical characteristics

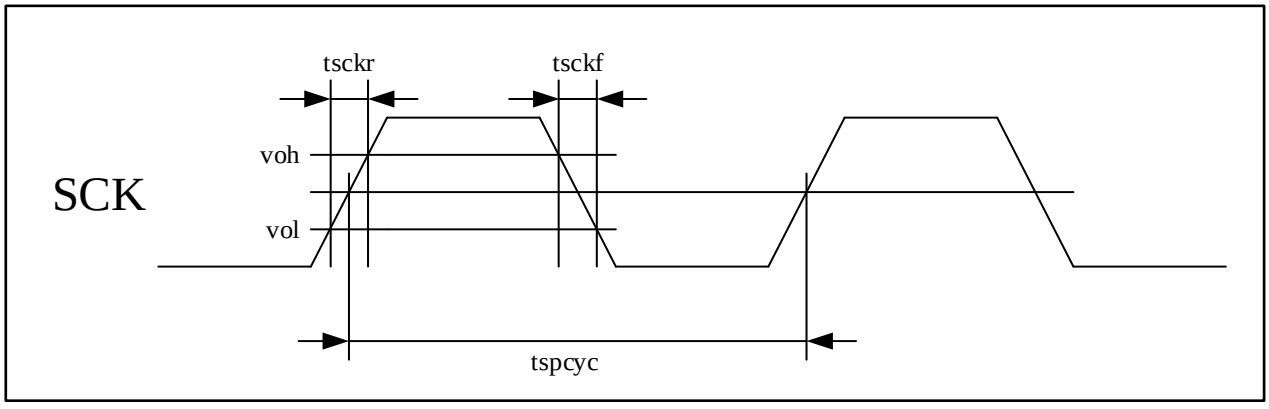


Figure3 -12 SCK Clock definition

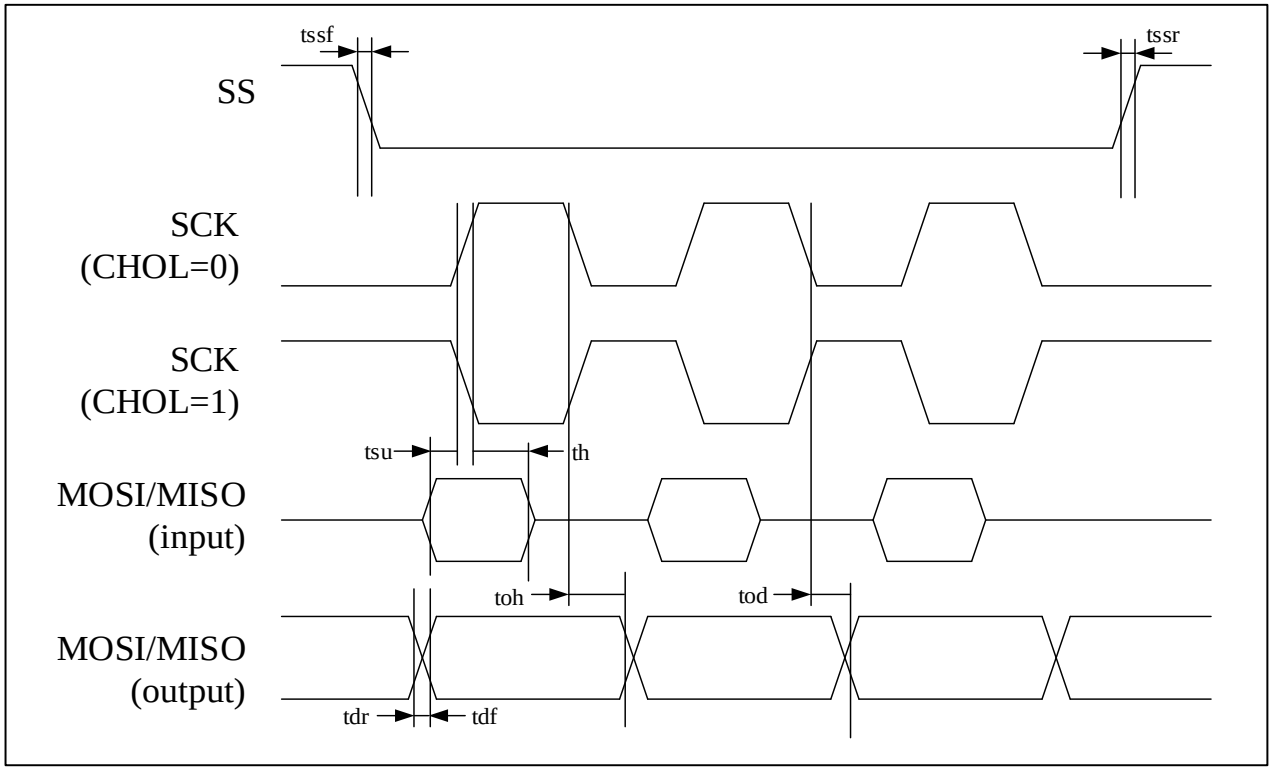


Figure3 -13 SPI interface timing requirements

3.3.12 CAN2.0B interface characteristics

For the port characteristics of CANx_TX and CANx_RX, please refer to 3.3.7I/O port characteristics .

3.3.13 USB interface characteristics

Symbol		Parameter	Conditions	Min (1)	Typ	Max (1)	Unit
Input	VCC	Operating Voltage	-	3.0 (2)	-	3.6	V
	V_{IL}	Input low level	-	-	-	0.8	V
	V_{IH}	Input high level	-	2.0	-	-	V
	V_{DI}	Differential input sensitivity	-	0.2	-	-	V
	V_{CM}	Differential common mode voltage	-	0.8	-	2.5	V
Output	V_{OL} (3)	Static output low level	R_L =1.5kΩ to 3.6V (4)	-	-	0.3	V
	V_{OH} (3)	Static output high level	R_L =15kΩ to VSS (4)	2.8	-	3.6	V
	V_{CRS}	Cross-over voltage	C_L =50pF	1.3	-	2.0	V
	t_R	Rise Time	C_L =50pF, 10%~90% of $\|V_{OH}-V_{OL}\|$	4	-	20	ns
	t_F	Fall time	C_L =50pF, 10%~90% of $\|V_{OH}-V_{OL}\|$	4	-	20	ns
	t_{RFMA}	Rise and fall time ratio t_R/t_F	C_L =50pF	90	-	111.1	%
R_{PD} (3)		Pull-down resistor	$V_{IN}=V_{CC}$, in host mode	14.25	-	24.80	kΩ
R_{PU} (3)		Pull-up resistance	$V_{IN}=V_{SS}$, idle state	0.900	1.2	1.575	kΩ
			$V_{IN}=V_{SS}$, in device mode	1.425	2.3	3.090	kΩ

Table3-25 USB Full-Speed electrical characteristics

1. All voltages are measured based on the local ground potential.
2. When the operating voltage drops to 2.7V, the function of the USB full-speed transceiver can still be

guaranteed, but the complete USB full-speed electrical characteristics cannot be guaranteed. The latter will degrade in the VCC voltage range of 2.7 to 3.0V.

3. Guarantee of mass production test.
4. $_{RL}$ is the load connected to the USB full-speed drive.

Symbol		Parameter	Conditions	Min (1)	Typ	Max (1)	Unit
Input	V_{CC}	Operating Voltage	-	3.0 (2)	-	3.6	V
	V_{IL}	Input low level	-	-	-	0.8	V
	V_{IH}	Input high level	-	2.0	-	-	V
	V_{DI}	Differential input sensitivity	-	0.2	-	-	V
	V_{CM}	Differential common mode voltage	-	0.8	-	2.5	V
Output	V_{OL} (3)	Static output low level	R_L =1.5kΩ to 3.6V (4)	-	-	0.3	V
	V_{OH} (3)	Static output high level	R_L =15kΩ to VSS (4)	2.8	-	3.6	V
	V_{CRS} (3)	Cross-over voltage	C_L =200pF~600pF	1.3	-	2.0	V
	t_R (3)	Rise Time	C_L =200pF~600pF, 10%~90% of $\|V_{OH}-V_{OL}\|$	75	-	300	ns
	t_F (3)	Fall time	C_L =200pF~600pF, 10%~90% of $\|V_{OH}-V_{OL}\|$	75	-	300	ns
	t_{RFMA} (3)	Rise and fall time ratio t_R/t_F	C_L =200pF~600pF	80	-	125	%
R_{PD} (3)		Pull-down resistor	$V_{IN}=V_{CC}$, in host mode	14.25	-	24.80	kΩ

Table3 -26 USB Low-Speed electrical characteristics

1. All voltages are measured based on the local ground potential.
2. When the operating voltage drops to 2.7V, the function of the USB low-speed transceiver can still be guaranteed, but the complete USB low-speed electrical characteristics cannot be guaranteed. The latter will deteriorate in the V_{CC} voltage range of 2.7 to 3.0V.
3. Guarantee of mass production test.
4. R_L is the load connected to the USB low-speed drive.

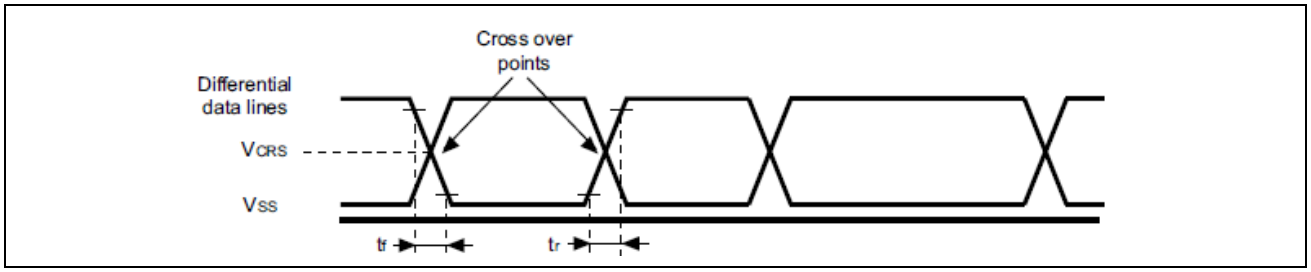


Figure3-14 USB rise/fall time and Cross Over voltage definition

3.3.14 PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL PFD(Phase Frequency Detector) input clock (1)	-	1	-	25	MHz
f_{PLL_OUT}	PLL multiplier output clock	-	15	-	240	MHz
f_{VCO_OUT}	PLL VCO output	-	240	-	480	MHz
$Jitter_{PLL}$	Period Jitter	PLL PFD input clock=8MHz, System clock=120MHz, Peak-to-Peak	-	±100	-	ps
	Cycle-to-Cycle Jitter	PLL PFD input clock=8MHz, System clock=120MHz, Peak-to-Peak	-	±150	-	
t_{LOCK}	PLL lock time	-	-	80	120	μs

Table3 - 27 PLL main performance indicators

1. It is recommended to use a higher input clock to obtain good Jitter characteristics.

3.3.15 JTAG interface characteristics

Synbol	Item	Min	Typ	Max	Unit
t_{TCKcyc}	JTCK clock cycle time	50	-	-	ns
t_{TCKH}	JTCK clock high pulse width	20	-	-	ns
t_{TCKL}	JTCK clock low pulse width	20	-	-	ns
t_{TCKr}	JTCK clock rise time	-	-	5	ns
t_{TCKf}	JTCK clock fall time	-	-	5	ns
t_{TMSs}	JTMS setup time	8	-	-	ns
t_{TMSh}	JTMS hold time	8	-	-	ns
t_{TDIs}	JTDI setup time	8	-	-	ns
t_{TDIh}	JTDI hold time	8	-	-	ns
t_{TDOd}	JTDO data delay time	-	-	20	ns

Table3 -28 JTAG interface characteristics

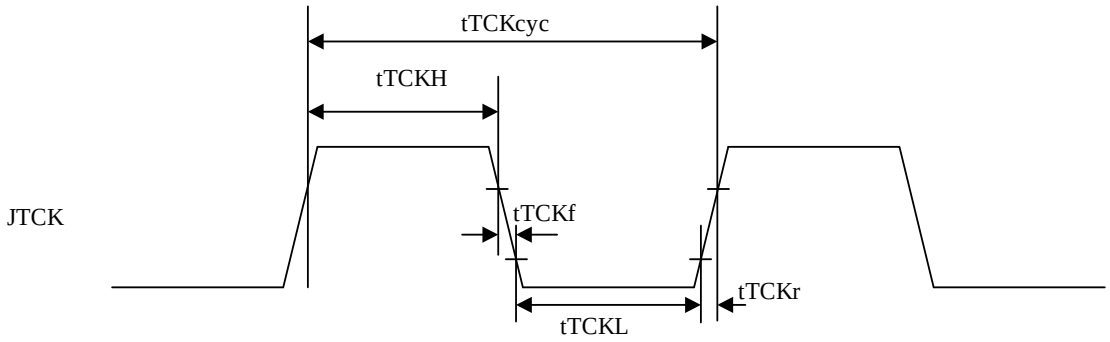


Figure3 - 15 JTAG JTCK clock

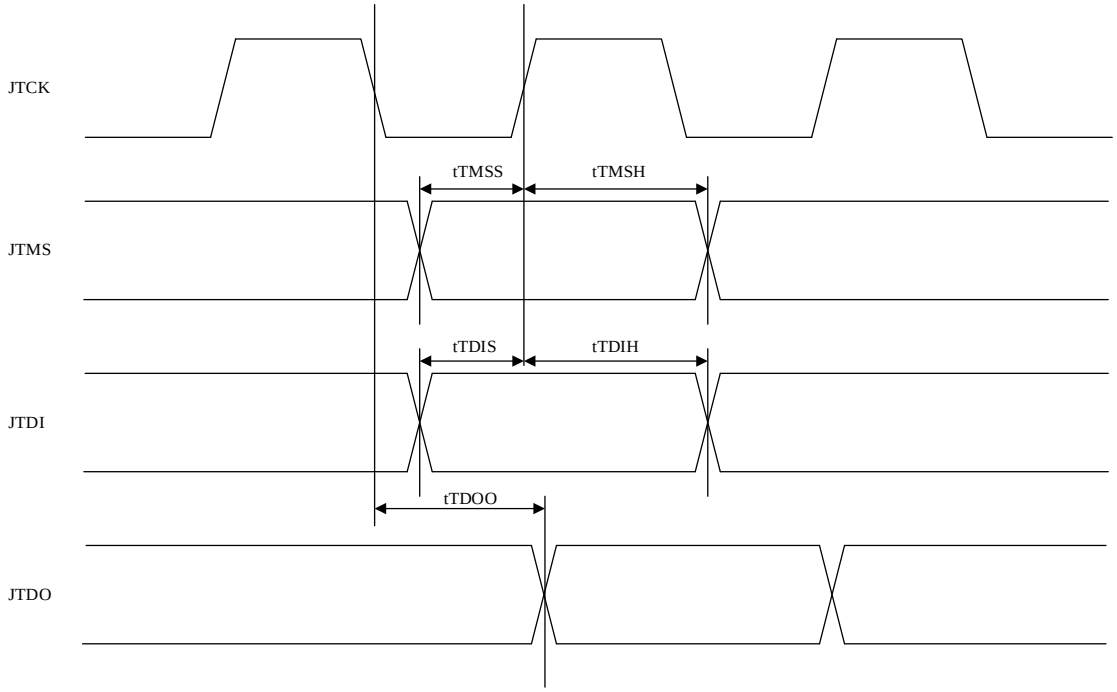


Figure3 -16 JTAG input and output

3.3.16 External timer characteristic

3.3.16.1 High-speed external subscriber clock generated by external source

In bypass mode, XTAL oscillator is off and the input pin is standard I/O. External clock signals must take into account I/O static characteristics.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{XTAL_EXT}	User external timer frequency	-	1	-	25	MHz
V_{IH_XTAL}	XTAL_IN input pin high level		$0.8*V_{CC}$	-	VCC	V
V_{IL_XTAL}	XTAL_IN input pin low level		VSS	-	$0.2*V_{CC}$	
$t_{r(XTAL)}$ $t_{f(XTAL)}$	XTAL_IN rise or fall time		-	-	5	ns
$Duty_{(XTAL)}$	Duty ratio	-	40	-	60	%

Table3 -29 High-speed external user clock characteristics

3.3.16.2 High-speed external clock produced by crystal oscillator/ceramic resonator

High-speed external (XTAL) clocks can be produced using a 4 to 25 MHz crystal oscillator/ceramic resonator oscillator. In applications, the resonator and load capacitance must be as close to the oscillator pin as possible to minimize output distortion and vibration stabilization time. For more information on the resonator characteristics (frequency, encapsulation, accuracy, etc.), please consult the crystal resonator manufacturer.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{XTAL_IN}	Oscillator frequency		4	-	25	MHz
R_F (1)	Feedback resistance		-	300	-	kΩ
A_{XTAL} (2)	XTAL accuracy	-	-500	-	500	ppm
G_{mmax}	Oscillator G_m	Wake up	4	-	-	mA/V
$t_{SU(XTAL)}$ (3)	Start time	VCC is stable, crystal oscillator = 8MHz	-	-	2.0	ms
		VCC is stable, crystal oscillator = 4MHz	-	-	4.0	ms

Table3 -30 XTAL 4-25 MHz oscillator characteristics

1. Guarantee of mass production test.
2. This parameter depends on the resonator used in the application system.
3. TSU (XTAL) is the start-up time, that is, the time between the software enabling the XTAL to measure until the stable 8MHz oscillation frequency is obtained. This value is measured based on the standard crystal resonator and may vary significantly with the crystal resonator manufacturer.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors designed for high-frequency applications that can meet the requirements of crystal oscillators or resonators (see the figure below). The size of C_{L1} and C_{L2} are usually the same, $C_{L1}=C_{L2}=2*(C_L-Cs)$. Cs is the stray capacitance of PCB and MCU pins (XTAL_IN, XTAL_OUT).

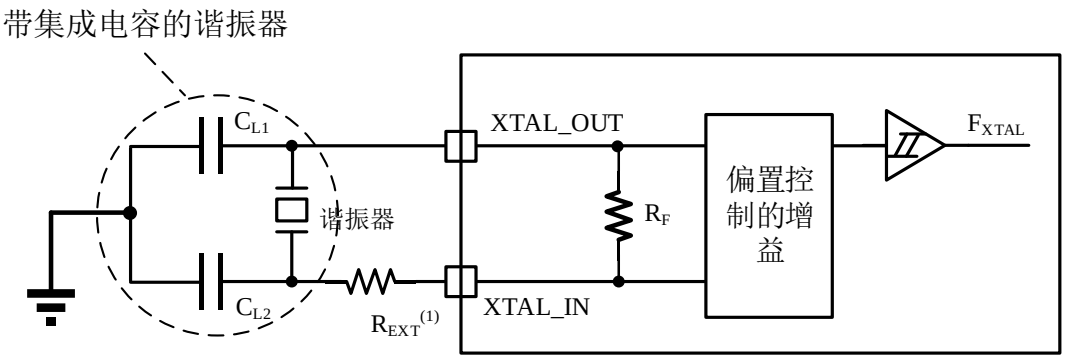


Figure3-17 Typical application with 8 MHz crystal oscillator

1. The value of REXT depends on the crystal oscillator characteristics.

3.3.16.3 Low-speed external clock generated by crystal oscillator/ceramic resonator

The low-speed external clock can be generated using an oscillator composed of a 32.768 kHz crystal/ceramic resonator. In applications, the resonator and load capacitance must be as close to the oscillator pin as possible to minimize output distortion and vibration stabilization time. For more information on the resonator characteristics (frequency, encapsulation, accuracy, etc.), please consult the crystal resonator manufacturer.

Symbol	Parameter	Conditions	Specifications			Unit
			Min	Typ	Max	
F_{XTAL32}	Frequency	-	-	32.768	-	kHz
R_F (1)	Feedback resistance	-	-	15	-	MΩ
I_{DD_XTAL32}	Power consumption	XTAL32DRV[2:0]=000	-	0.8	-	μA
A_{XTAL32} (2)	XTAL32 accuracy	-	-500	-	500	ppm
G_{mmax}	Oscillator G_m	-	5.6	-	-	uA/V
$T_{SUXTAL32}$	At startup between (3)	VCC steady state	-	2	-	s

Table3 - 31 XTAL32 oscillator characteristics

1. Guarantee of mass production test.
2. This parameter depends on the resonator used in the application system.
3. TSUXTAL 32 is the start-up time, which starts with the software enabling XTAL 32 to measure until

a stable oscillation frequency of 32.768 kHz is obtained. This value is measured based on the standard crystal resonator and may vary significantly with the crystal resonator manufacturer.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors (see the figure below). The size of C_{L1} and C_{L2} are usually the same, $C_{L1}=C_{L2}=2*(C_L-Cs)$. Cs is the stray capacitance of PCB and MCU pins (XTAL32_IN, XTAL32_OUT). If C_{L1} and C_{L2} are greater than 18pF, it is recommended to set XTAL32DRV[2:0]=001 (large drive, the typical value of power consumption increases by 0.2uA).

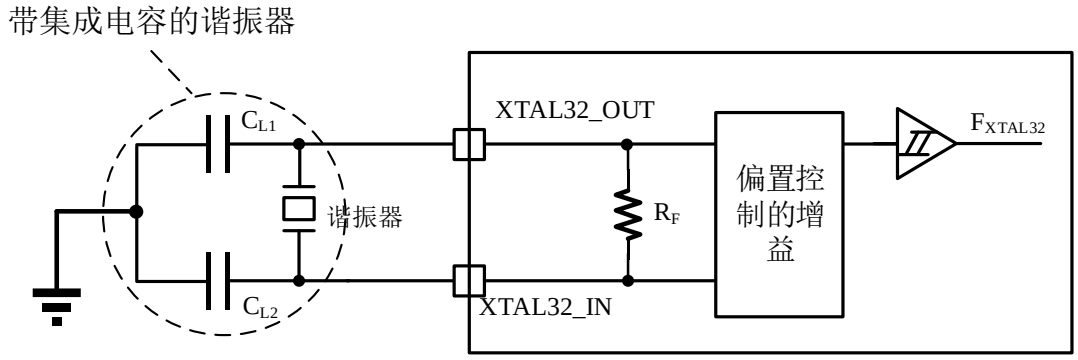


Figure3 - 18 Typical application with 32.768 kHz crystal oscillator

3.3.17 Internal timer characteristics

3.3.17.1 Internal High Speed (HRC) oscillator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HRC}	Frequency (1)	Pattern 1	-	16	-	MHz
		Pattern 2	-	20	-	
	User adjusts the	-	-	-	0.2	%
	Frequency accuracy (1)	T_A = -40 to 105 ℃	-2	-	2	%
		T_A = -20 to 105 ℃	-1.5	-	1.5	%
		T_A = 25 ℃	-0.5	-	0.5	%
$t_{st(HRC)}$	HRC oscillator	-	-	-	15	μs

Table3-32 HRC oscillator characteristics

1. Guarantee of mass production test.

3.3.17.2 Internal Medium Speed (MRC) Oscillator

Symbol	Parameter	Min	Typ	Max	Unit
f_{MRC} (1)	Frequency	7.2	8	8.8	MHz
$t_{st(MRC)}$	MRC oscillator stabilization time	-	-	3	μs

Table3 - 33 MRC oscillator characteristics

1. Guarantee of mass production test.

3.3.17.3 Internal Low Speed (LRC) oscillator

Symbol	Parameter	Min	Typ	Max	Unit
f_{LRC} (1)	Frequency	27.853	32.768	37.683	kHz
$t_{st(LRC)}$	LRCoscillator Stabilization Time	-	-	36	μs

Table3- 34 LRC oscillator characteristics

1. Guarantee of mass production test.

3.3.17.4 SWDT dedicated internal low-speed (SWDTLRC) oscillator

Symbol	Parameter	Min	Typ	Max	Unit
$f_{SWDTLRC}$ (1)	Frequency	9	10	11	kHz
tst(SWDTLRC)	SWDTLRC oscillator stabilization time	-	-	57.1	μs

Table3 - 35 SWDTLRC oscillator characteristics

1. Guarantee of mass production test.

3.3.18 12-bit ADC characteristic

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{AVCC}	Power supply	-	1.8	-	3.6	V
V_{REFH} (1)	Positive reference voltage	-	1.8	-	V_{AVCC}	V
f_{ADC}	ADC conversion clock frequency	Ultra-high speed/high-speed action mode V_{AVCC} =2.4 ~3.6V	1	-	60	MHz
		Ultra-high speed/high-speed action mode V_{AVCC} =1.8 ~2.4V	1	-	30	
		Ultra low speed action mode	1	-	8	
V_{AIN}	Conversion voltage range	-	V_{AVSS}	-	V_{REFH}	V
R_{AIN}	External input impedance	Refer to Formula 1 for details	-	-	50	kΩ
R_{ADC}	Sampling switch resistance	-	-	-	6	kΩ
C_{ADC}	Internal sampling and retention capacitance	-	-	4	7	pF
t_D	Trigger conversion delay	f_{ADC} = 60 MHz	-	-	0.3	μs

Table3 -36 ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_S	Sampling time	f_{ADC} =60MHz	0.183	-	4.266	μs
			11	-	255	1/ f_{ADC}
t_{CONV}	Single-channel total conversion time (Including sampling time)	f_{ADC} = 60 MHz 12 bit resolution	0.4	-	-	μs
		f_{ADC} = 60 MHz 10-bit resolution	0.36	-	-	μs
		f_{ADC} = 60 MHz 8-bit resolution	0.33	-	-	μs
		20 to 268 (sampling time tS + successive approach n-bit resolution + +1)				1/f_{ADC}
f_S	Sampling rate f_{ADC} = 60 MHz	12-bit resolution single ADC	-	-	2.5	Msps
		12-bit resolution time interpolation dual ADC	-	-	4.6	
t_{ST}	Power-on time	-	-	1	2	μs

Table3-37 ADC characteristics (continued)

1. V_{AVCC} -V_{REFH} <1.2V

Formula 1: RAIN Maximum Formula

$$R_{AIN} = \frac{k-1}{f_{ADC}\ X\ C_{ADC}\ X \ln(2^{N+2})} - R_{ADC}$$

The above formula (Formula 1) is used to determine the maximum external impedance to make the error lower than 1/4 LSB. Where N = 12 (12 bit resolution), k is the number of sampling cycles defined in the ADC _ SSTR register.

Symbol	Parameter	Conditions	Typ	Max	Unit
E_T	Absolute error	Ultra-high speed/high-speed action mode f_{ADC} =60MHz Input source impedance < 1 kΩ V_{AVCC} =2.4 ~3.6V	±4.5	±6	LSB
E_O	Offset error		±3.5	±6	LSB
E_G	Gain error		±3.5	±6	LSB
E_D	Differential linear error		±1	±2	LSB
E_L	Integral linear error		±1.5	±3	LSB

Table3-38 ADC1_IN0~3, ADC12_IN4~IN7 input channel accuracy @ f_{ADC} =60MHz

Symbol	Parameter	Conditions	Typ	Max	Unit
E_T	Absolute error	Ultra-high speed/high-speed action mode f_{ADC} =30MHz Input source impedance < 1 kΩ V_{AVCC} =2.4 ~3.6V	±4.5	±6	LSB
E_O	Offset error		±3.5	±6	LSB
E_G	Gain error		±3.5	±6	LSB
E_D (1)	Differential linear error		±1	±2	LSB
E_L (1)	Integral linear error		±1.5	±3	LSB

Table3 - 39 ADC1_IN0~3, ADC12_IN4~IN7 input channel accuracy @ f_{ADC} =30MHz

1. Guarantee of mass production test.

Symbol	Parameter	Conditions	Typ	Max	Unit
E_T	Absolute error	Ultra-high speed/high-speed action mode f_{ADC} =30MHz Input source impedance < 1 kΩ V_{AVCC} =1.8 ~2.4V	±4.5	±6	LSB
E_O	Offset error		±3.5	±6	LSB
E_G	Gain error		±3.5	±6	LSB
E_D	Differential linear error		±1	±2	LSB
E_L	Integral linear error		±2	±3	LSB

Table3 - 40 ADC1_IN0~3, ADC12_IN4~IN7 input channel accuracy @ f_{ADC} =30MHz

Symbol	Parameter	Conditions	Typ	Max	Unit
E_T	Absolute error	In ultra-low speed action mode f_{ADC} =8MHz Input source impedance < 1 kΩ V_{AVCC} =1.8 ~3.6V	±4.5	±6	LSB
E_O	Offset error		±3.5	±6	LSB
E_G	Gain error		±3.5	±6	LSB
E_D	Differential linear error		±1	±2	LSB
E_L	Integral linear error		±2	±3	LSB

Table3-41 ADC1_IN0~3, ADC12_IN4~IN7 input channel accuracy @ f_{ADC} =8MHz

Symbol	Parameter	Conditions	Typ	Max	Unit
E_T	Absolute error	Ultra-high speed/high-speed action mode f_{ADC} =60MHz Input source impedance < 1 kΩ V_{AVCC} =2.4 ~3.6V	±5.5	±7	LSB
E_O	Offset error		±4.5	±7	LSB
E_G	Gain error		±4.5	±7	LSB
E_D	Differential linear error		±1.5	±2	LSB
E_L	Integral linear error		±2.0	±3	LSB

Table3-42 ADC1_IN12~15, ADC12_IN8~11 input channel accuracy @ f_{ADC} =60MHz

Symbol	Parameter	Conditions	Typ	Max	Unit
E_T	Absolute error	Ultra-high speed/high-speed action mode f_{ADC} =30MHz Input source impedance < 1 kΩ V_{AVCC} =2.4 ~3.6V	±5.5	±7	LSB
E_O	Offset error		±4.5	±7	LSB
E_G	Gain error		±4.5	±7	LSB
E_D (1)	Differential linear error		±1.5	±2	LSB
E_L (1)	Integral linear error		±2.0	±3	LSB

Table3 - 43 ADC1_IN12~15, ADC12_IN8~11 input channel accuracy @ f_{ADC} =30MHz

1. Guarantee of mass production test.

Symbol	Parameter	Conditions	Typ	Max	Unit
E_T	Absolute error	Ultra-high speed/high-speed action mode f_{ADC} =30MHz Input source impedance < 1 kΩ V_{AVCC} =1.8 ~2.4V	±5.5	±7	LSB
E_O	Offset error		±4.5	±7	LSB
E_G	Gain error		±4.5	±7	LSB
E_D	Differential linear error		±1.5	±2	LSB
E_L	Integral linear error		±2.5	±3	LSB

Table3-44 ADC1_IN12~15, ADC12_IN8~11 input channel accuracy @ f_{ADC} =30MHz

Symbol	Parameter	Conditions	Typ	Max	Unit
E_T	Absolute error	In ultra-low speed action mode f_{ADC} =8MHz Input source impedance < 1 kΩ V_{AVCC} =1.8 ~3.6V	±5.5	±7	LSB
E_O	Offset error		±4.5	±7	LSB
E_G	Gain error		±4.5	±7	LSB
E_D	Differential linear error		±1.5	±2	LSB
E_L	Integral linear error		±2.5	±3	LSB

Table3 -45 ADC1_IN12~15, ADC12_IN8~11 input channel accuracy @ f_{ADC} =8MHz

Symbol	Parameter	Conditions	Min	Max	Unit
ENOB	Effective digits	Ultra-high speed/high-speed action mode f_{ADC} =60MHz Input signal frequency = 2kHz Input source impedance < 1 kΩ V_{AVCC} =2.4 ~3.6V	10.6	-	Bits
SINAD	Signal-to-noise harmonic ratio		64	-	dB
SNR	Signal-to-noise ratio		66	-	dB
THD	Total harmonic distortion		-	-70	dB

Table3 - 46 ADC1_IN0~3, ADC12_IN4~IN7 input channel input channel dynamic accuracy @ f_{ADC} =60MHz

Symbol	Parameter	Conditions	Min	Max	Unit
ENOB	Effective digits	Ultra-high speed/high-speed action mode f_{ADC} =30MHz Input signal frequency = 2kHz Input source impedance < 1 kΩ V_{AVCC} =1.8~2.4V	10.4	-	Bits
SINAD	Signal-to-noise harmonic ratio		62	-	dB
SNR	Signal-to-noise ratio		64	-	dB
THD	Total harmonic distortion		-	-67	dB

Table3-47 ADC1_IN0~3, ADC12_IN4~IN7 input channel input channel dynamic accuracy @ f_{ADC} =30MHz

Symbol	Parameter	Conditions	Min	Max	Unit
ENOB	Effective digits	In ultra-low speed action mode f_{ADC} =8MHz Input signal frequency = 2kHz Input source impedance < 1 kΩ V_{AVCC} =1.8~3.6V	10.4	-	Bits
SINAD	Signal-to-noise harmonic ratio		62	-	dB
SNR	Signal-to-noise ratio		64	-	dB
THD	Total harmonic distortion		-	-67	dB

Table3 -48 ADC1_IN0~3, ADC12_IN4~IN7 input channel input channel dynamic accuracy @ f_{ADC} =8MHz

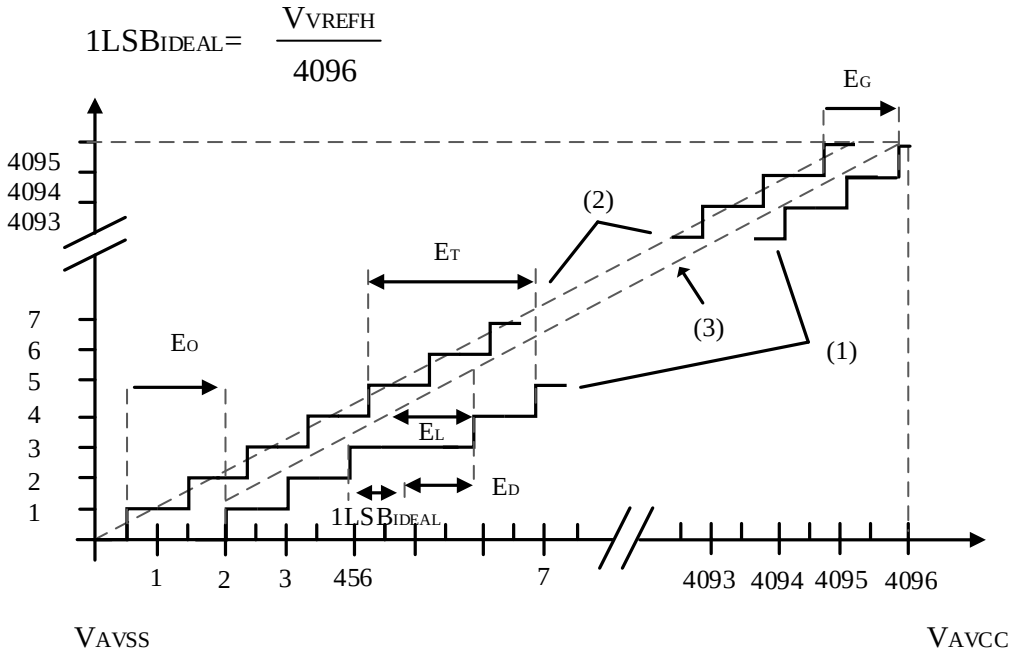


Figure3 -19 ADC accuracy characteristics

1. Refer to also table above.
2. Examples of actual transmission curves.
3. Ideal transfer curve.
4. End point correlation line.
5. E_T = total unadjusted error: The maximum deviation between actual and ideal transmission curves.

   E_O = Offset error: The deviation between the first actual conversion and the first ideal conversion.

   E_G = gain error: The deviation between the last ideal conversion and the last actual conversion.

   E_D = Differential linearity error: The maximum deviation between the actual step and the ideal value.

   E_L = integral linearity error: The maximum deviation between any actual conversion and the relative line of the endpoint.

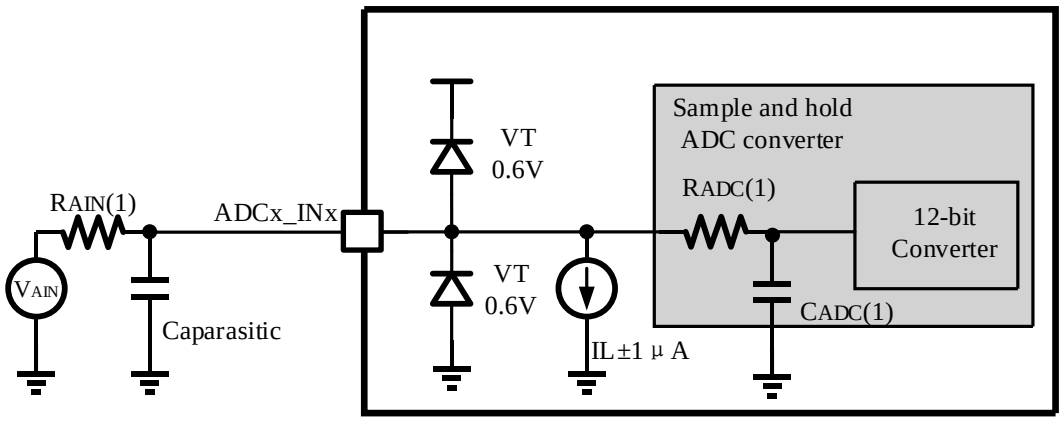


Figure3 -20 Typical connection using ADC

1. About R_{AIN} , R_{ADC} And C_{ADC} Value information, seeTable3 -36 .
2. Cparasitic represents PCB capacitance (depending on welding and PCB wiring quality) and pad capacitance (approximately 5 pF). Higher Cparasitic value will result in lower conversion accuracy. To solve this problem, you should reduce f_{ADC} .

General PCB design guidelines

The power supply should be decoupled as shown in the figure below, depending on whether VREFH is connected to AVCC and the number of AVCC pins. 0.1μ The F capacitor should be a (high-quality) ceramic capacitor. These capacitors should be as close as possible to the chip.

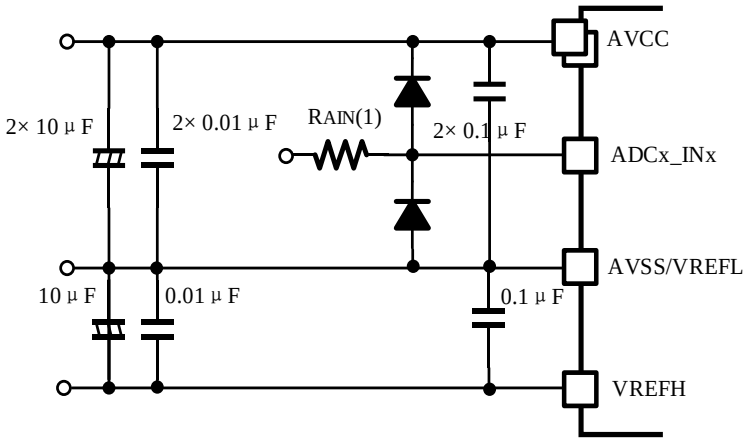


Figure3 -21 Power supply and reference power supply decoupling example

3.3.19 DAC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{AVCC}	Analog supply voltage	-	1.8	3.3	3.6	V
DNL	Differential non-linearity error (deviation between two consecutive	-	-	-	±2	LSB
Offset	Offset error (the difference between the measured value at the	-	-	-	±2	LSB
$T_{SETTLING}$	Setup time (full scale: Suitable for 8-digit input code conversion between the lowest input code and the highest input code when	-	-	-	8	μs

Table3 - 49 DAC characteristics

3.3.20 Comparator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{AVCC}	Analog supply voltage	-	1.8	3.3	3.6	V
V_I	Input voltage range	-	0	-	V_{AVCC}	V
T_{cmp}	Comparison time	Comparator resolution	-	50	100	ns
T_{set}	Input channel switching	-	-	100	200	ns

Table3 - 50 Comparator features

3.3.21 Gain adjustable amplifier characteristics

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{AVCC}	Analog supply voltage		-	1.8	3.3	3.6	V
V_{OS} (1)	Input offset voltage		-	-8	-	8	mV
V_I	Input voltage range		-	0.1*V_{AVCC} /Gain	-	0.9*V_{AVCC} /Gain	V
G_E	Gain error	Use external port PGAVSS as PGA negative phase input	Gain=2 (1)	-1	-	1	%
			Gain=2.133	-1	-	1	%
			Gain=2.286	-1	-	1	%
			Gain=2.667	-1	-	1	%
			Gain=2.909	-1	-	1	%
			Gain=3.2	-1.5	-	1.5	%
			Gain=3.556	-1.5	-	1.5	%
			Gain=4.0	-1.5	-	1.5	%
			Gain=4.571	-2	-	2	%
			Gain=5.333	-2	-	2	%
			Gain=6.4	-3.0	-	3.0	%
			Gain=8	-3.0	-	3.0	%
			Gain=10.667	-4.0	-	4.0	%
			Gain=16	-4.0	-	4.0	%
			Gain=32 (1)	-7.0	-	7.0	%
		Use the internal analog ground AVSS as the negative phase input of the PGA	Gain=2 (1)	-2	-	2	%
			Gain=2.133	-2	-	2	%
			Gain=2.286	-2	-	2	%
			Gain=2.667	-2	-	2	%
			Gain=2.909	-2	-	2	%
			Gain=3.2	-2.5	-	2.5	%
			Gain=3.556	-2.5	-	2.5	%
			Gain=4.0	-2.5	-	2.5	%

			Gain=4.571	-3.0	-	3.0	%
			Gain=5.333	-3.0	-	3.0	%
			Gain=6.4	-4.0	-	4.0	%
			Gain=8	-4.0	-	4.0	%
			Gain=10.667	-5.0	-	5.0	%
			Gain=16	-5.0	-	5.0	%
			Gain=32 (1)	-8.0	-	8.0	%

Table3 - 51 Gain adjustable amplifier characteristics

1. Guarantee of mass production test.

3.3.22 Temperature Sensor

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_L	Relative	According to the user manual, each	-	-	±5	℃

Table3 - 52 Temperature sensor characteristics

3.3.23 Memory characteristics

3.3.23.1 Flash memory

Flash memory was erased when the device was delivered to the customer.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{VCC}	Supply current	Read mode, V_{CC} =1.8 V~3.6V	-	-	5	mA
		Programming mode, V_{CC} =1.8 V~3.6V	-	-	10	
		Block erase mode, V_{CC} =1.8 V~3.6V	-	-	10	
		Full erase mode, V_{CC} =1.8 V~3.6V	-	-	10	

Table3 -53 Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{prog} (1)	Word	Single programming	43+2* T_{hclk}(2)	48+4* T_{hclk}(2)	53+6* T_{hclk}(2)	μs
	Word	Continuous	12+2* T_{hclk}(2)	14+4* T_{hclk}(2)	16+6* T_{hclk}(2)	μs
T_{erase} (1)	Block erase time	-	16+2* T_{hclk}(2)	18+4* T_{hclk}(2)	20+6* T_{hclk}(2)	ms
T_{mas} (1)	Full erase time	-	16+2* T_{hclk}(2)	18+4* T_{hclk}(2)	20+6* T_{hclk}(2)	ms

Table3 -54 Flash memory programming and erasing time

1. Guarantee of mass production test.
2. Thclk is one cycle of CPU clock.

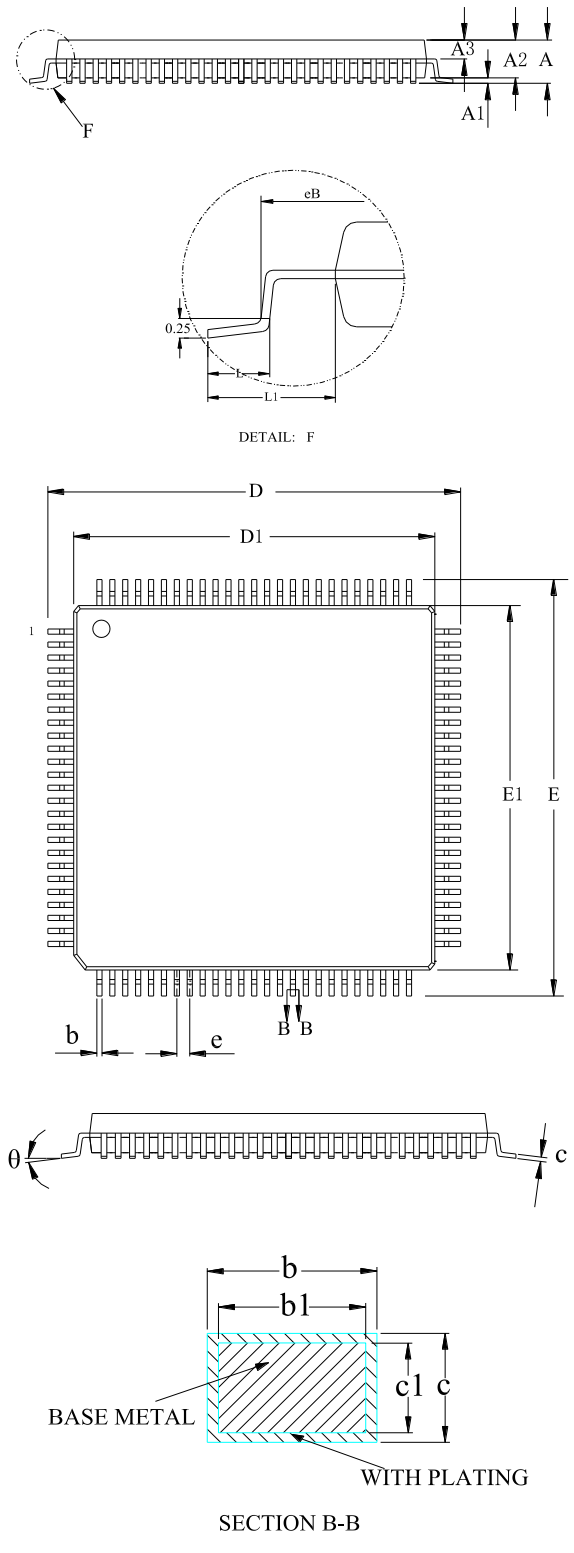
Symbol	Parameter	Conditions	Min	Unit
N_{end}	Programming, number of block erases	T_A = 85°C	10	kcycles
N_{end}	Number of whole erases	T_A = 85°C	10	kcycles
T_{ret}	Data retention period	T_A = 85°C, after 10 kcycles	10	Years

Table3 -55 Flash memory erasable times and data retention period

4 Package information

4.1 Package size

LQFP100 package

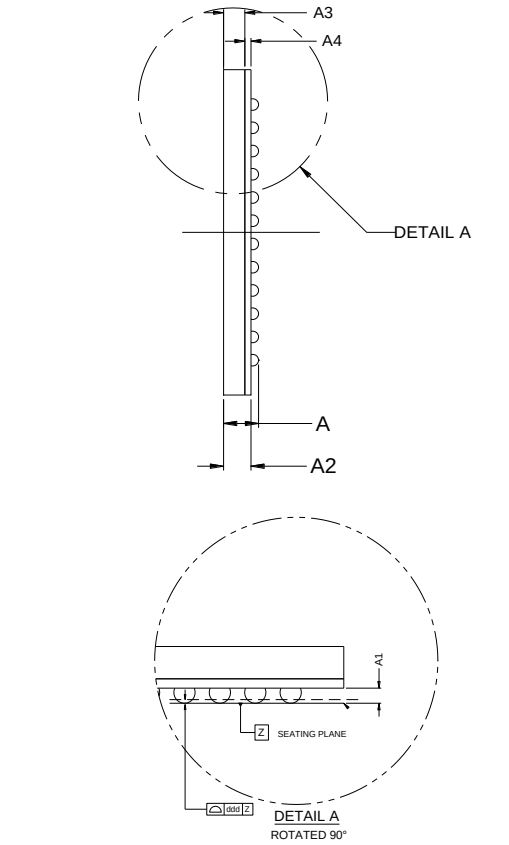


Symbol	14x14 Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.26
b1	0.17	0.20	0.23
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
e	0.50BSC		
L	0.45	-	0.75
L1	1.00REF		
θ	0	-	7°

NOTE:

- **Dimensions “D1” and “E1” do not include mold flash.**

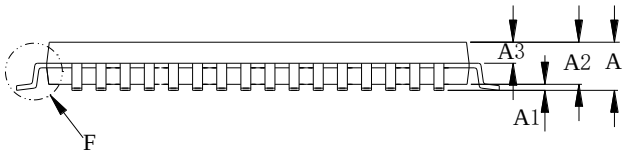
VFBGA100 package

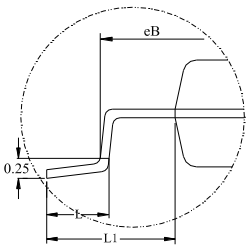


BOTTOM VIEW

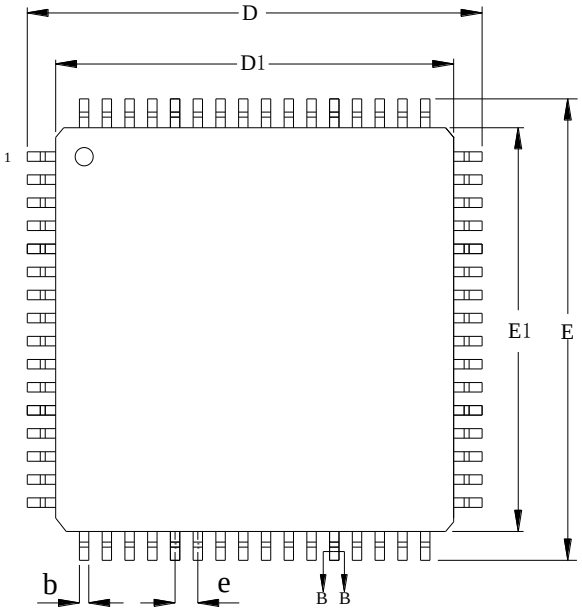
Symbol	7x7 Millimeter		
	Min	Nom	Max
A	0.67	0.74	0.81
A1	0.11	0.16	0.21
A2	0.54	0.58	0.62
A3		0.45REF	
A4		0.13REF	
b	0.20	0.25	0.30
D	6.90	7.00	7.10
D1	-	5.5	-
E	6.90	7.00	7.10
E1	-	5.5	-
e	-	0.5	-
F		0.75REF	
ddd	-	0.10	-
eee	-	0.15	-
fff	-	0.05	-

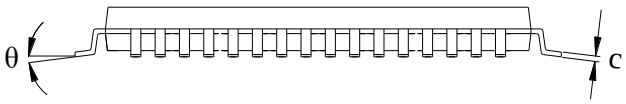
LQFP64 package

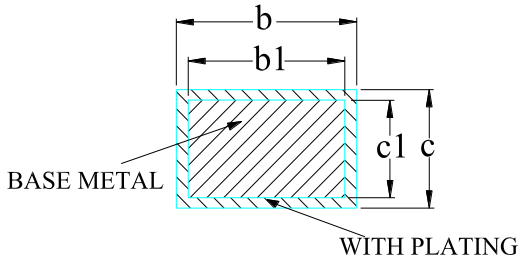




DETAIL: F







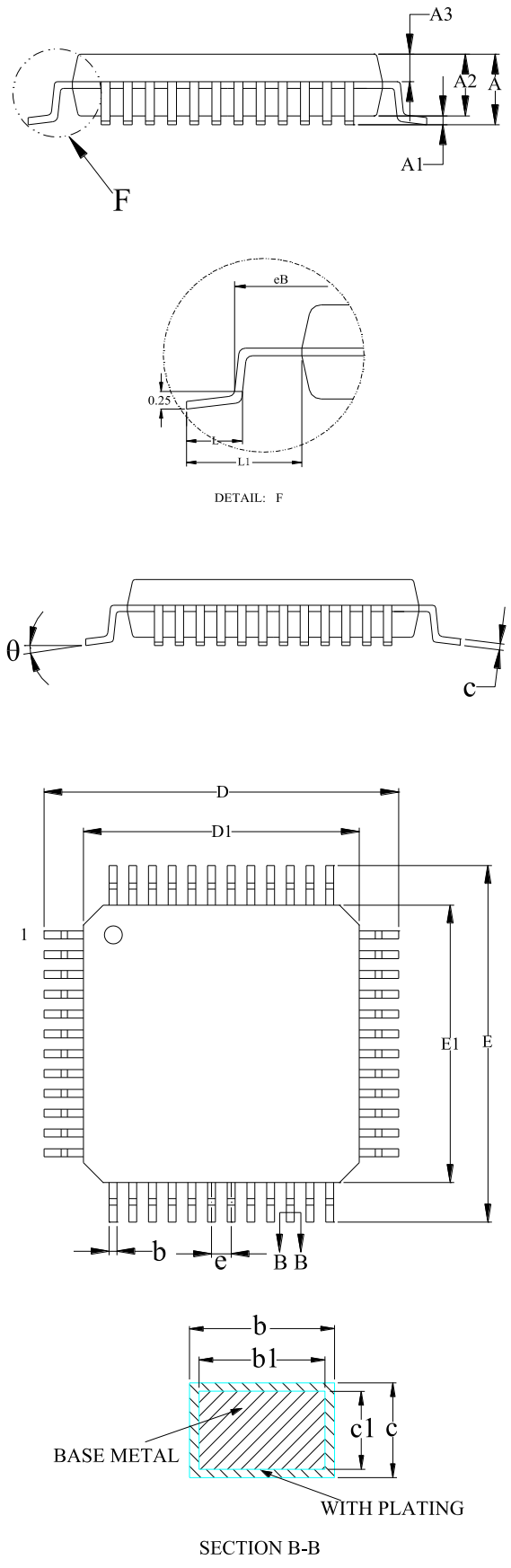
SECTION B-B

Symbol	10x10 Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.26
b1	0.17	0.20	0.23
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	0.50BSC		
L	0.45	-	0.75
L1	1.00REF		
θ	0°	-	7°

NOTE:

- **Dimensions “D1” and “E1” do not include mold flash.**

LQFP48 package

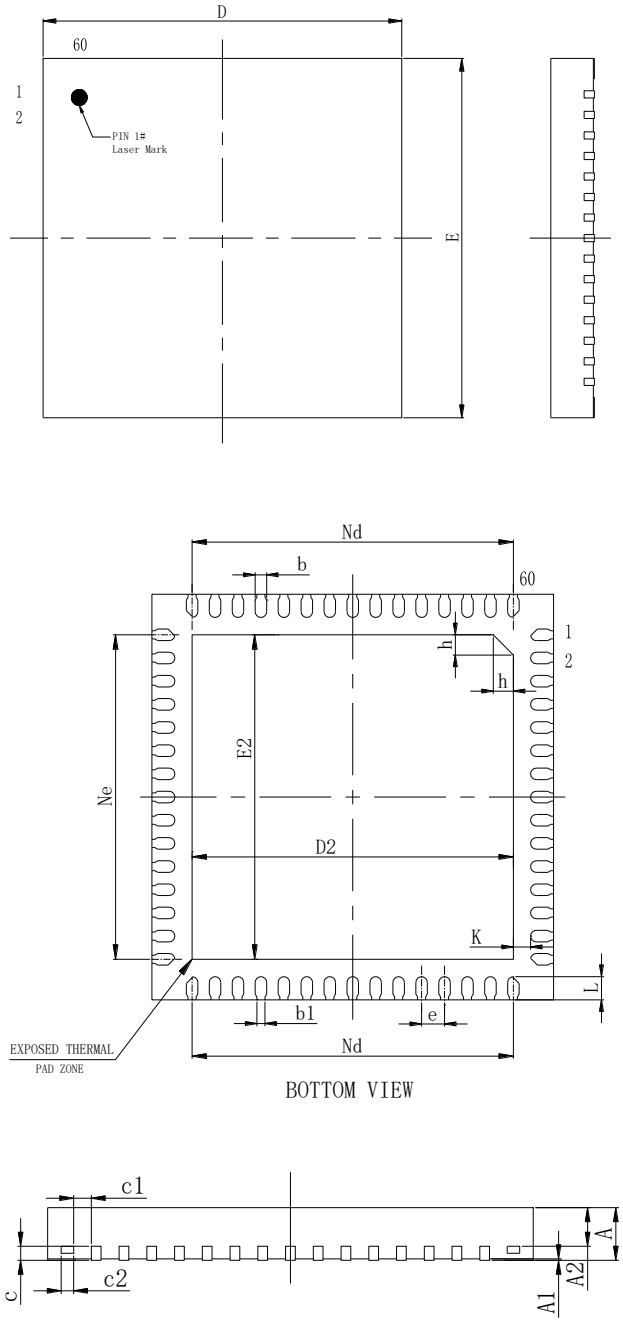


Symbol	7x7 Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.26
b1	0.17	0.20	0.23
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.50BSC		
L	0.40	-	0.65
L1	1.00REF		
θ	0	-	7°

NOTE:

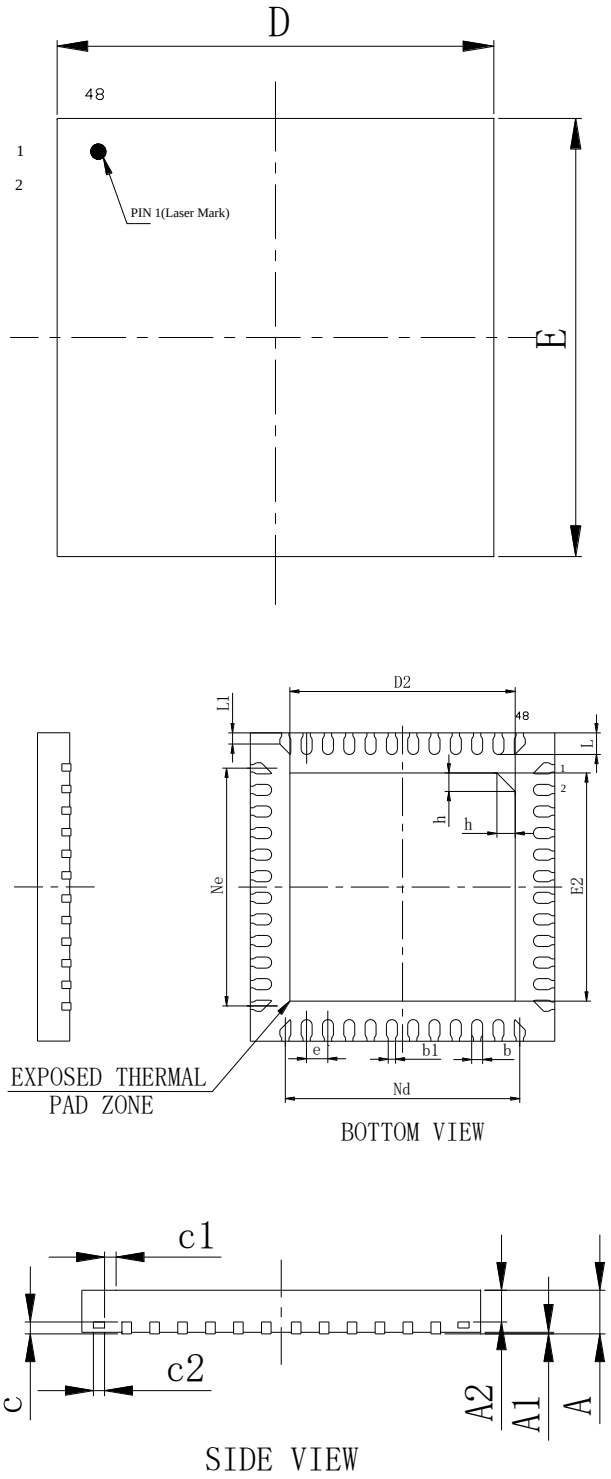
- **Dimensions “D1” and “E1” do not include mold flash.**

QFN60 package



Symbol	7x7 Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2		0.547REF	
b	0.15	0.20	0.25
b1		0.14REF	
c		0.20REF	
c1		0.255RE F	
c2		0.18REF	
D	6.90	7.00	7.10
D2	5.50	5.60	5.70
Nd		5.60BSC	
e		0.40BSC	
E	6.90	7.00	7.10
E2	5.50	5.60	5.70
Ne		5.60BSC	
L	0.35	0.40	0.45
K	0.25	0.30	0.35
h	0.30	0.35	0.40

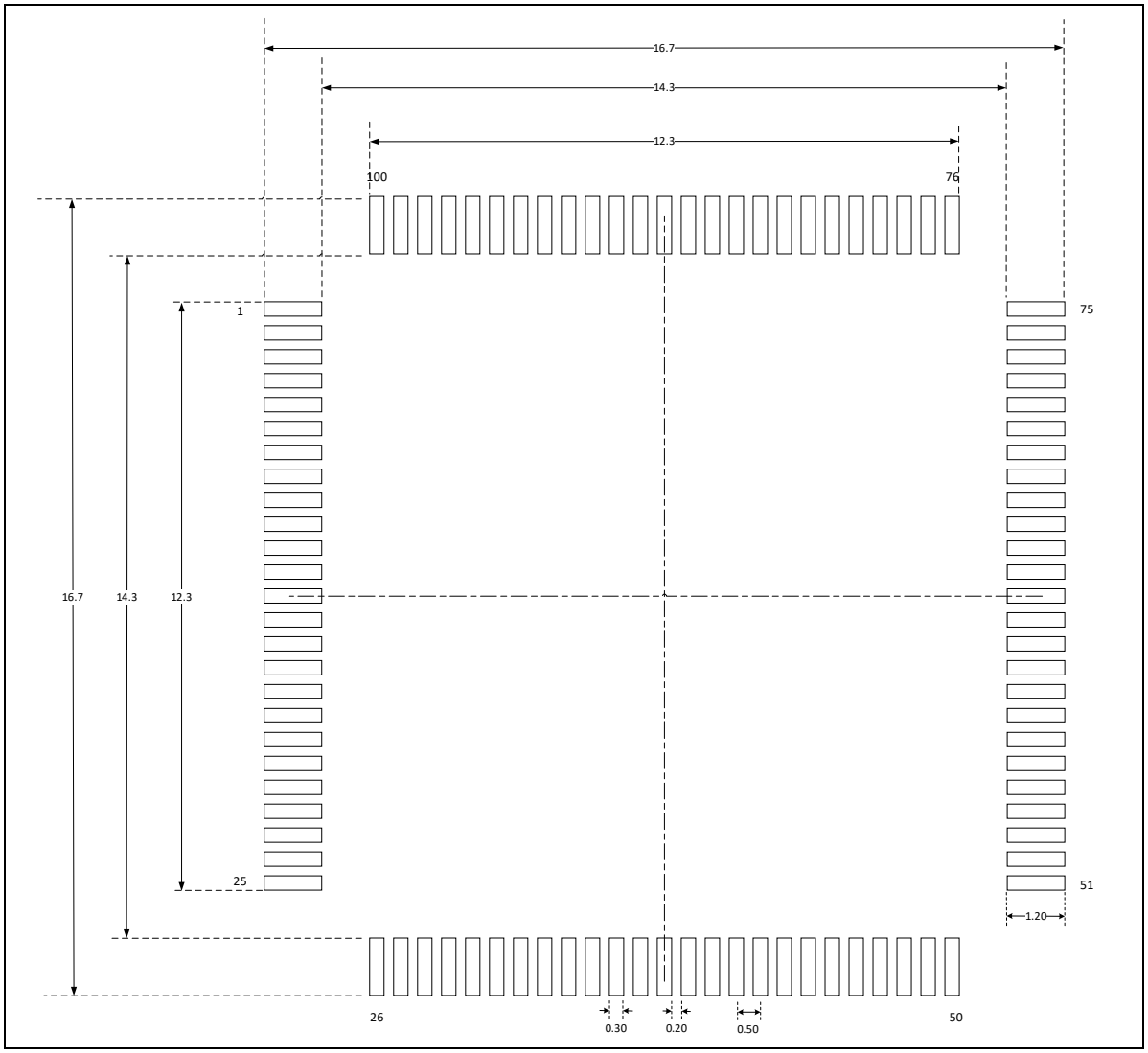
QFN48 package



Symbol	5x5 Millimeter		
	Min	Nom	Max
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A2		0.40REF	
b	0.13	0.18	0.23
b1		0.12REF	
c	0.10	0.15	0.20
c1		0.145REF	
c2		0.140REF	
D	4.90	5.00	5.10
D2	3.60	3.70	3.80
e		0.35BSC	
Ne		3.85BSC	
Nd		3.85BSC	
E	4.90	5.00	5.10
E2	3.60	3.70	3.80
L	0.30	0.35	0.40
L1	0.13	0.18	0.23
h	0.25	0.30	0.35
L/F carrier size		154 x 154	

4.2 Schematic diagram of the pad

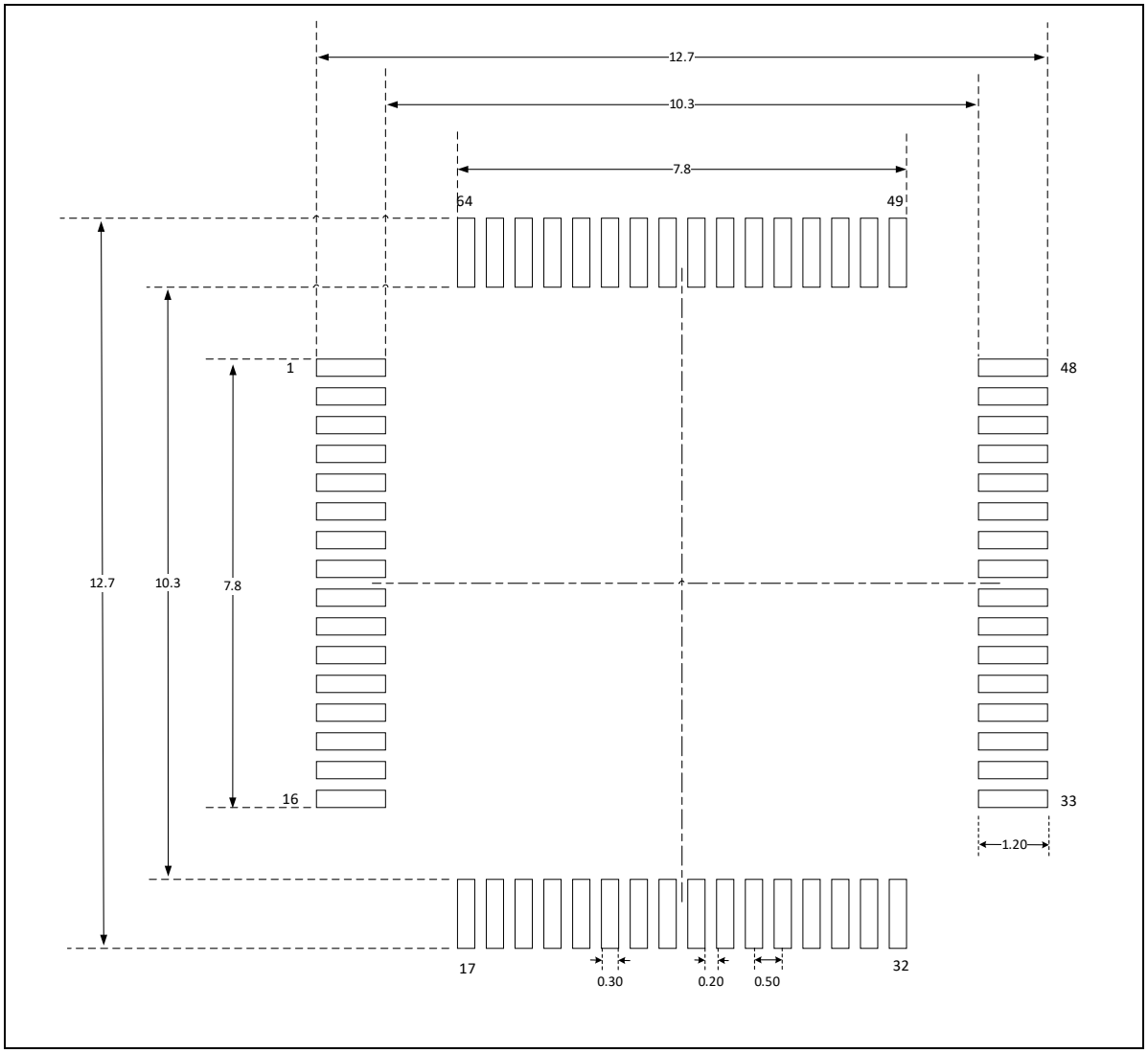
LQFP100 package (14mm x 14mm)



NOTE:

- **Dimensions are expressed in millimeters.**
- **Dimensions are for reference only.**

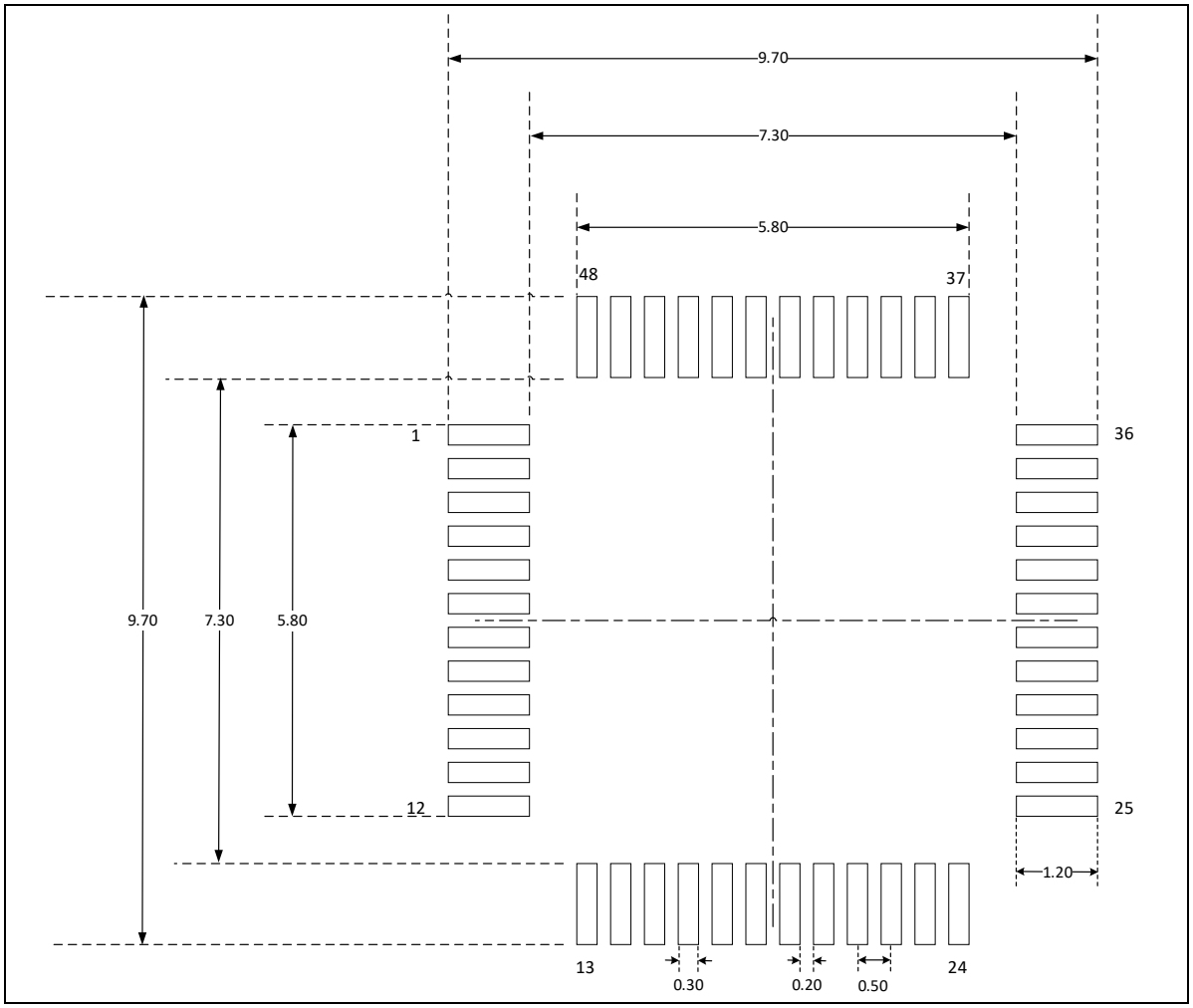
LQFP64 package (10mm x 10mm)



NOTE:

- **Dimensions are expressed in millimeters.**
- **Dimensions are for reference only.**

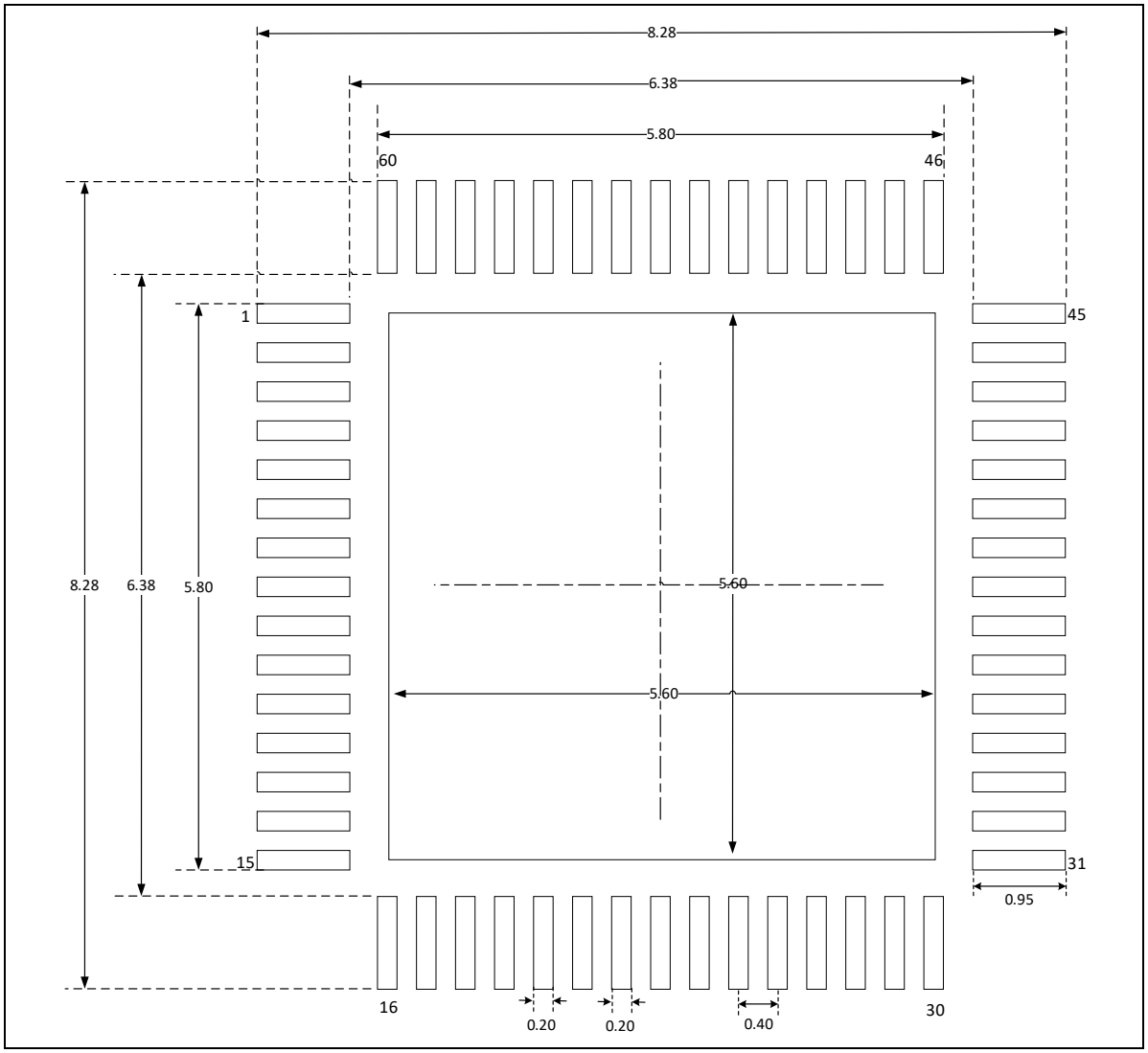
LQFP48 package （7mm x 7mm）



NOTE:

- **Dimensions are expressed in millimeters.**
- **Dimensions are for reference only.**

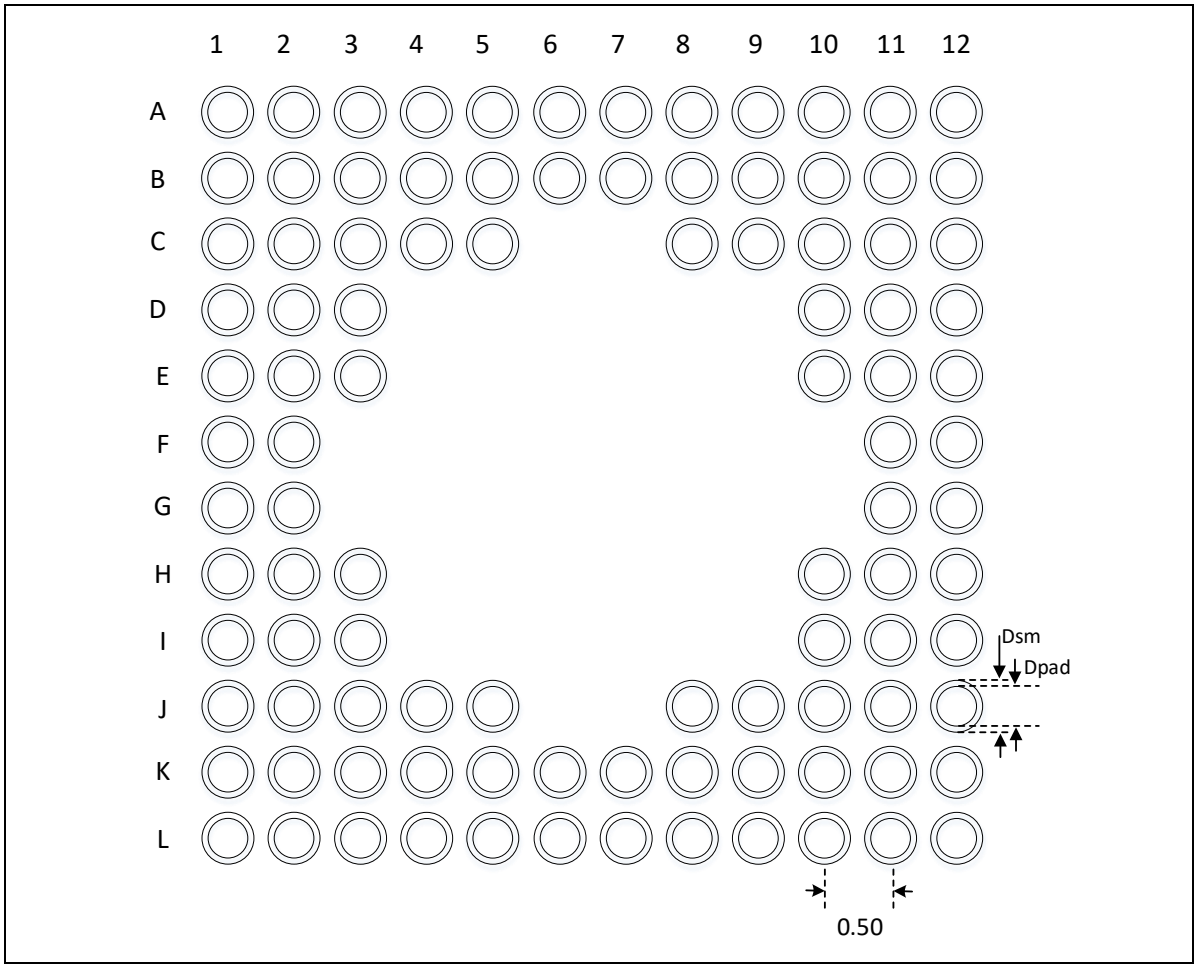
QFN60 package (7mm x 7mm)



NOTE:

- **Dimensions are expressed in millimeters.**
- **Dimensions are for reference only.**

VFBGA100 package (7mm x 7mm)



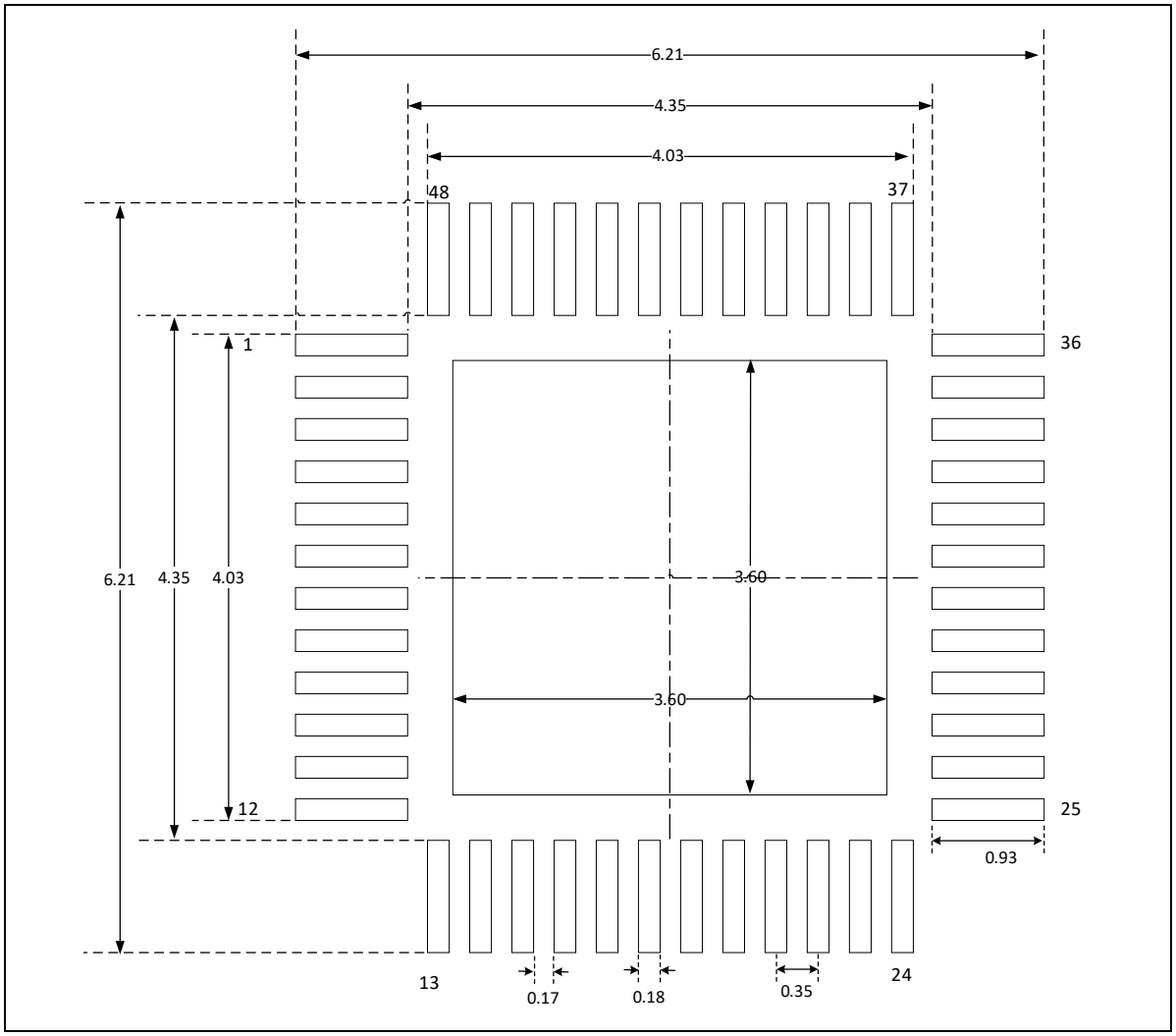
NOTE:

- **Dimensions are expressed in millimeters.**
- **Dimensions are for reference only.**

VBGA100 recommended PCB design rules(0.5mm pitch)

Dimension	Recommended values
Pitch	0.5mm
Dpad	0.240mm
Dsm	0.340mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.240mm
Stencil thickness	Between 0.100mm and 0.125mm

QFN48 package (5mm x 5mm)



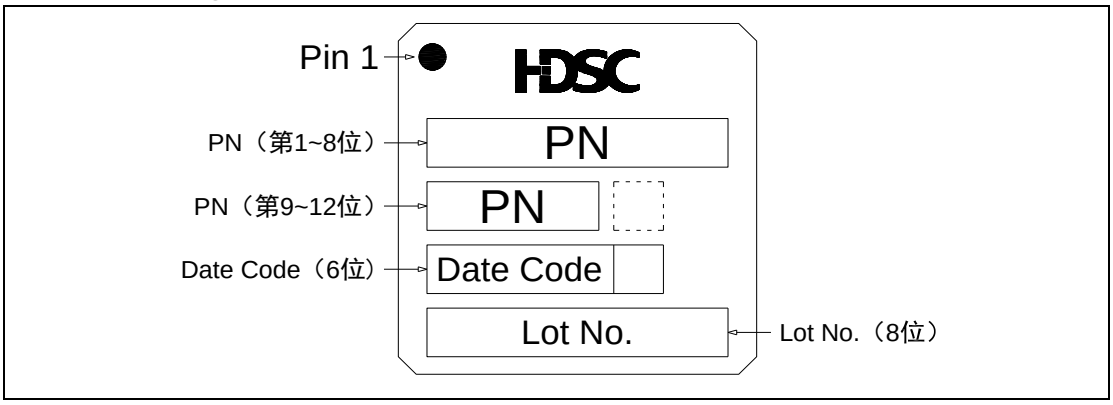
NOTE:

- **Dimensions are expressed in millimeters.**
- **Dimensions are for reference only.**

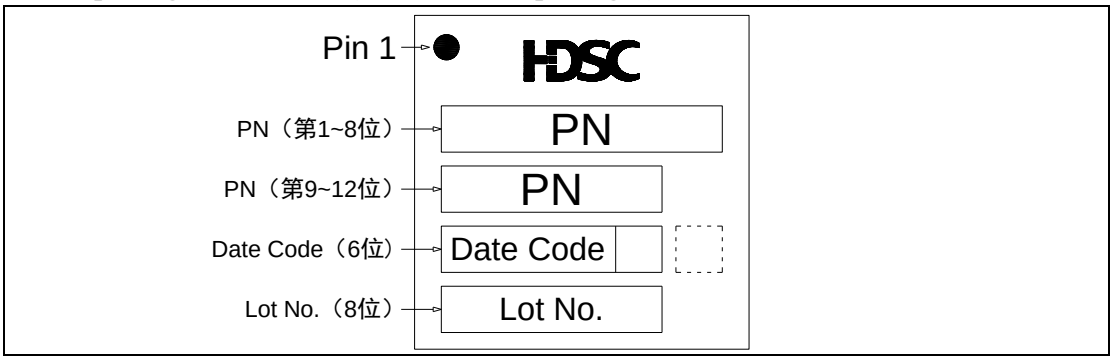
4.3 Silkscreen instructions

The position and information of Pin 1 printed on the front of each package are given below.

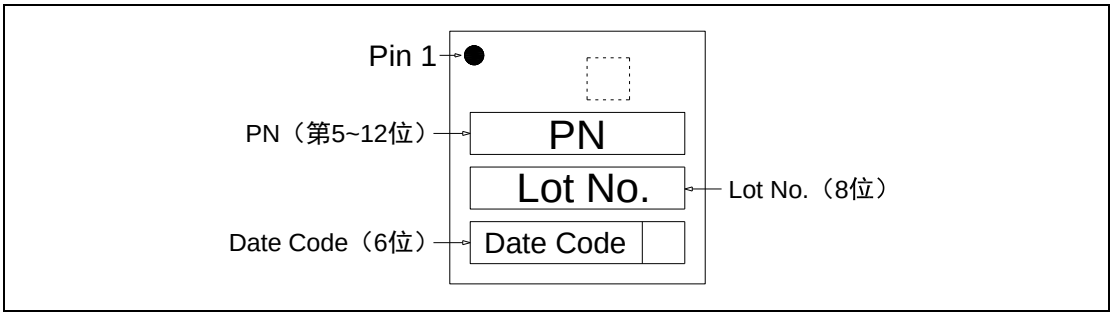
LQFP100 Package (14mm x 14mm) / LQFP64 Package (10mm x 10mm)
LQFP48 package （7mm x 7mm）



QFN60 package (7mm x 7mm) / VFBGA100 package (7mm x 7mm)



QFN48 package (5mm x 5mm)



Note:

- The blank boxes in the above figure indicate optional marks related to production, which are not explained in this section.

4.4 Package thermal resistance coefficient

When the packaged chip is working at the specified working environment temperature, the junction temperature Tj (℃) of the chip table can be calculated according to the following formula:

$$T_j = T_{amb} + (P_D \times \theta_{JA})$$

- T_{amb} refers to the working environment temperature when the packaged chip is working, the unit is ℃;
- θ_{JA} refers to the thermal resistance coefficient of the package to the working environment, the unit is ℃/W;
- $_{PD}$ is equal to the sum of internal power consumption of the chip and I/O power consumption, and the unit is W. The internal power consumption of the chip is the $I_{DD} \times V_{DD\ of\ the\ product}$. I/O power consumption refers to the power consumption generated by the I/O pins when the chip is working. Usually, the value of this part is very small and can be ignored.

The junction temperature $T_{j\ on\ the}$ table of the chip when the chip is operating at the specified operating ambient temperature must not exceed the maximum junction temperature T_J allowed by the chip.

Package Type and Size	Thermal Resistance Junction-ambient Value (θ_{JA})	Unit
LQFP100 14mm x 14mm / 0.5mm pitch	50 +/- 10%	℃/W
LQFP64 10mm x 10mm / 0.5mm pitch	65 +/- 10%	℃/W
LQFP48 7mm x 7mm / 0.5mm pitch	75 +/- 10%	℃/W
QFN60 7mm x 7mm / 0.4mm pitch	30 +/- 10%	℃/W
QFN48 5mm x 5mm / 0.35mm pitch	42 +/- 10%	℃/W

Table4 -1 Thermal resistance coefficient table of each package

5 Ordering Information

Part Number	HC32F460JEUA-QFN48TR	HC32F460JETA-LQFP48	HC32F460KEUA-QFN60TR	HC32F460KETA-LQFP64	HC32F460PETB-LQFP100	HC32F460PEHB-VFBGA100	HC32F460JCTA-LQFP48	HC32F460KCTA-LQFP64	HC32F460PCTB-LQFP100
Main frequency (MHz)	200	200	200	200	200	200	200	200	200
Core	ARM Cortex-M4	ARM Cortex-M4	ARM Cortex-M4	ARM Cortex-M4	ARM Cortex-M4	ARM Cortex-M4	ARM Cortex-M4	ARM Cortex-M4	ARM Cortex-M4
Flash (KB)	512	512	512	512	512	512	256	256	256
RAM (KB)	192	192	192	192	192	192	192	192	192
OTP (B)	960	960	960	960	960	960	960	960	960
Package (mm*mm)	QFN48 (5*5) e=0.35	LQFP48 (7*7) e=0.5	QFN60 (7*7) e=0.4	LQFP64 (10*10) e=0.5	LQFP100 (14*14) e=0.5	VFBGA100 (7*7) e=0.5	LQFP48 (7*7) e=0.5	LQFP64 (10*10) e=0.5	LQFP100 (14*14) e=0.5
GPIO	38	38	50	52	83	83	38	52	83
Voltage (V)	1.8~3.6	1.8~3.6	1.8~3.6	1.8~3.6	1.8~3.6	1.8~3.6	1.8~3.6	1.8~3.6	1.8~3.6
16-bit Timer	11	11	11	11	11	11	11	11	11
Motor control timer	3	3	3	3	3	3	3	3	3
12-bit ADC conversion unit	2	2	2	2	2	2	2	2	2
12-bit ADC channel number	10	10	15	16	16	16	10	16	16
Vcomp	3	3	3	3	3	3	3	3	3
PGA	1	1	1	1	1	1	1	1	1
SPI	4	4	4	4	4	4	4	4	4
QUADSPI	1	1	1	1	1	1	1	1	1
I^2S	4	4	4	4	4	4	4	4	4
I^2C	3	3	3	3	3	3	3	3	3
U(S)ART	4	4	4	4	4	4	4	4	4
CAN	1	1	1	1	1	1	1	1	1
SDIO	2	2	2	2	2	2	2	2	2
Full speed USB OTG	1	1	1	1	1	1	1	1	1
DMA	8	8	8	8	8	8	8	8	8
DCU	4	4	4	4	4	4	4	4	4
PVD	√	√	√	√	√	√	√	√	√
AES128	√	√	√	√	√	√	√	√	√
SHA256	√	√	√	√	√	√	√	√	√
TRNG	√	√	√	√	√	√	√	√	√
CRC	√	√	√	√	√	√	√	√	√
KEYSCAN	√	√	√	√	√	√	√	√	√
RTC	√	√	√	√	√	√	√	√	√
FLASH physical encryption	√	√	√	√	√	√	√	√	√
Packing	Tape reel	TRAY	Tape reel	TRAY	TRAY	TRAY	TRAY	TRAY	TRAY

Before ordering, please contact the sales window for the latest mass production information.

Version information & contact details

Version	Date	Summary of revised content
Rev1.0	2019/11/12	First edition release.
Rev1.1	2020/1/10	①Add 256KB product description to the full text; ②Add VFBGA package description to the full text; ③Electrical characteristics Revise the current max value of 105°C in power-down mode in the middle; ④update Silkscreen instructions .
Rev1.2	2020/8/26	1) Added description of ultra-high-speed operation mode, updated CoreMark/DMIPS, and added description of ultra-high-speed mode. Update the functional block diagram. 2) Pin configuration diagram Increase the 256KB model. 3) Increase Schematic diagram of the pad withPackage thermal resistance coefficient. 4) Added BOR/PVD characteristics and current characteristics in ultra-high-speed mode. 5) Update the JTAG/SWJ debug port pins.
Rev1.3	2021/12/10	Modify the statement,Package size Increase the A2/c1/c2 size of QFN48/60 in QFN48/60, modifyFlash memory Medium data retention period. Several specification changes. See the Chinese version of the datasheet for details.

If you have any comments or suggestions during the purchase and use process, please feel free to contact us.

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URL:http://www.hdsc.com.cn/mcu.htm

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